Wistron Confidential

PV

2009/10/19 REV :PV-01

<Variant Name>

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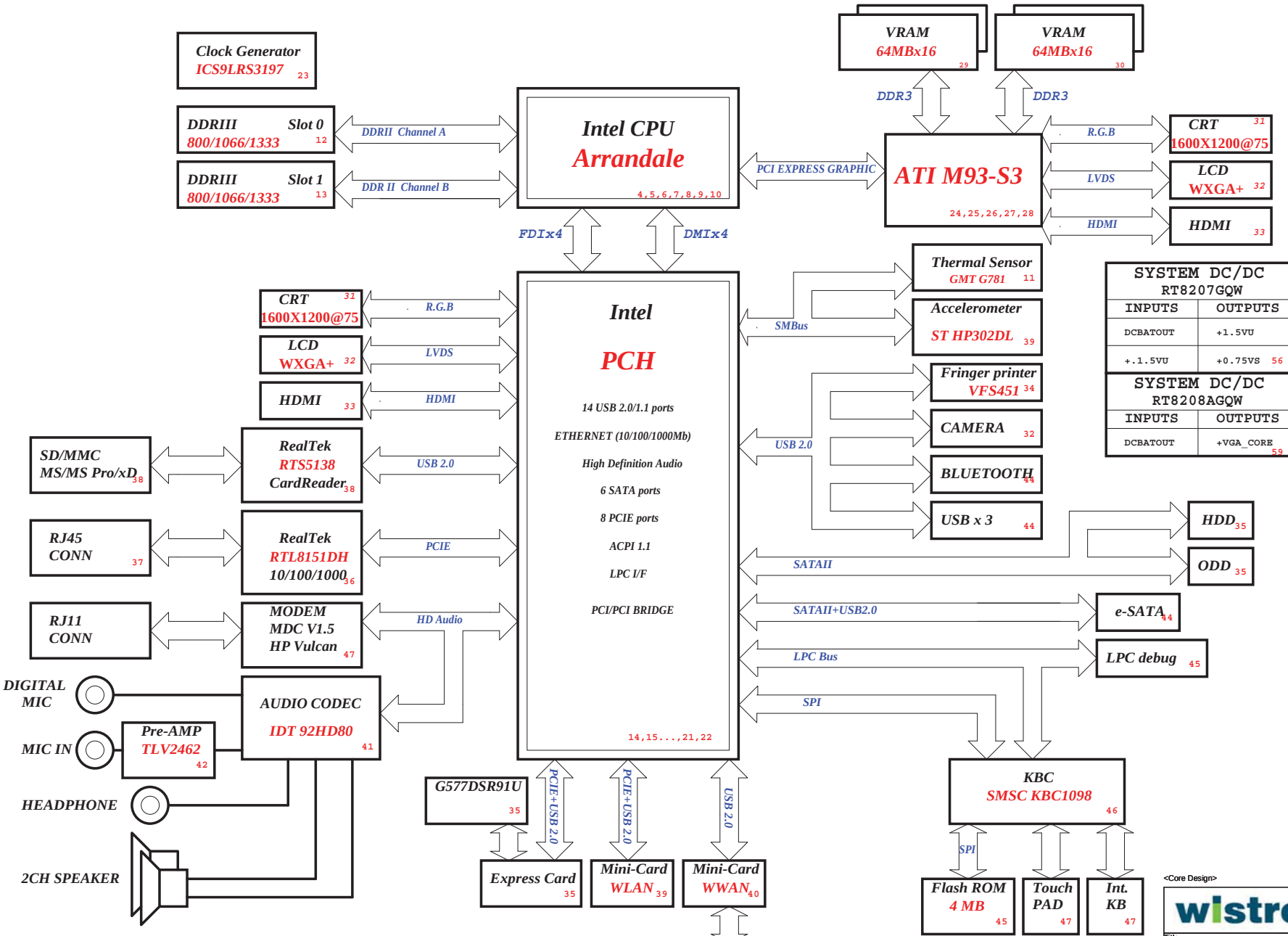
Title	S-Class Intel	
Size: A3	Document Number: S-Class Intel	Rev: SD
Date: Wednesday, October 28, 2009	Sheet 1 of 62	

Intel Calpella Arrandale Block Diagram



SYSTEM DC/DC RT8205A	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 53

SYSTEM DC/DC RT8209B	
INPUTS	OUTPUTS
DCBATOUT	+1.05VS_VTT +1.05VS 58

SYSTEM DC/DC ADP3211MNR2G	
INPUTS	OUTPUTS
DCBATOUT	+VCC_GFX_CORE 55

SYSTEM DC/DC RT8207GQW	
INPUTS	OUTPUTS
DCBATOUT	+1.5VU
+.1.5VU	+0.75VS 56

SYSTEM DC/DC RT8208AGQW	
INPUTS	OUTPUTS
DCBATOUT	+VGA_CORE 59

TI CHARGER BQ24740	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 52

CPU DC/DC ADP3212MNR2G	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 65A 54

SYSTEM DC/DC APL5930/APL5930	
INPUTS	OUTPUTS
+3VS	+1.8VS_NB +1.8VS_VGA
+1.5VS	+1.1V_REG 57

PCB 6 LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

<Core Design>

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Title: Block Diagram

Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 Sheet 2 of 62

PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing page 15

LANE2	EXP
LANE4	WLAN
LANE6	LAN

USB Table page 18

Pair	Device
0	External USB2
1	USB1 (Debug port)
2	ESATA USB4
3	Card Reader
4	NEW CARD
5	FREE
6	WLAN
7	FREE
8	BLUETOOTH
9	WWAN
10	Fingerprint
11	External USB3
12	CAMERA
13	FREE

091019-1

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

090901-1

SMBUS Control Table

	SOURCE	BATT	THERMAL SENSOR	CLK GEN	SODIMM	G-SENSOR	SMSC1098	M93
AB1A_DATA AB1A_CLK	SMSC1098	V	X	X	X	X	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	V	V
PCH_SMB_DATA PCH_SMB_CLK	Calpella	X	V	V	V	V	X	X

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Title: Notes List

Size: A3 | Document Number: S-Class Intel | Rev: SD

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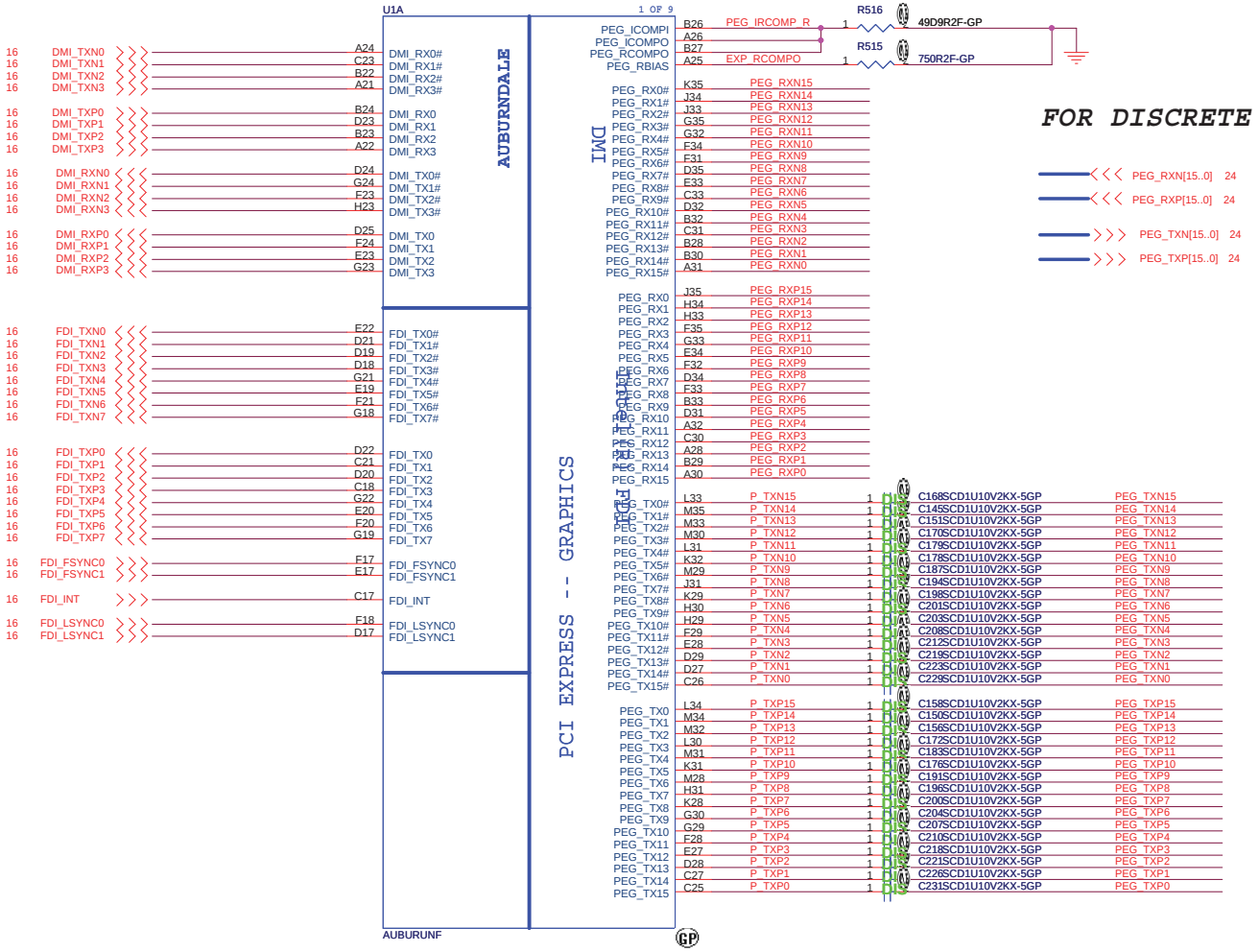
CPU(1/7)



<Core Design>

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Title: CPU (1/7)-PEG / DMI / FDI

Size	Document Number	Rev
A3	S-Class Intel	SD

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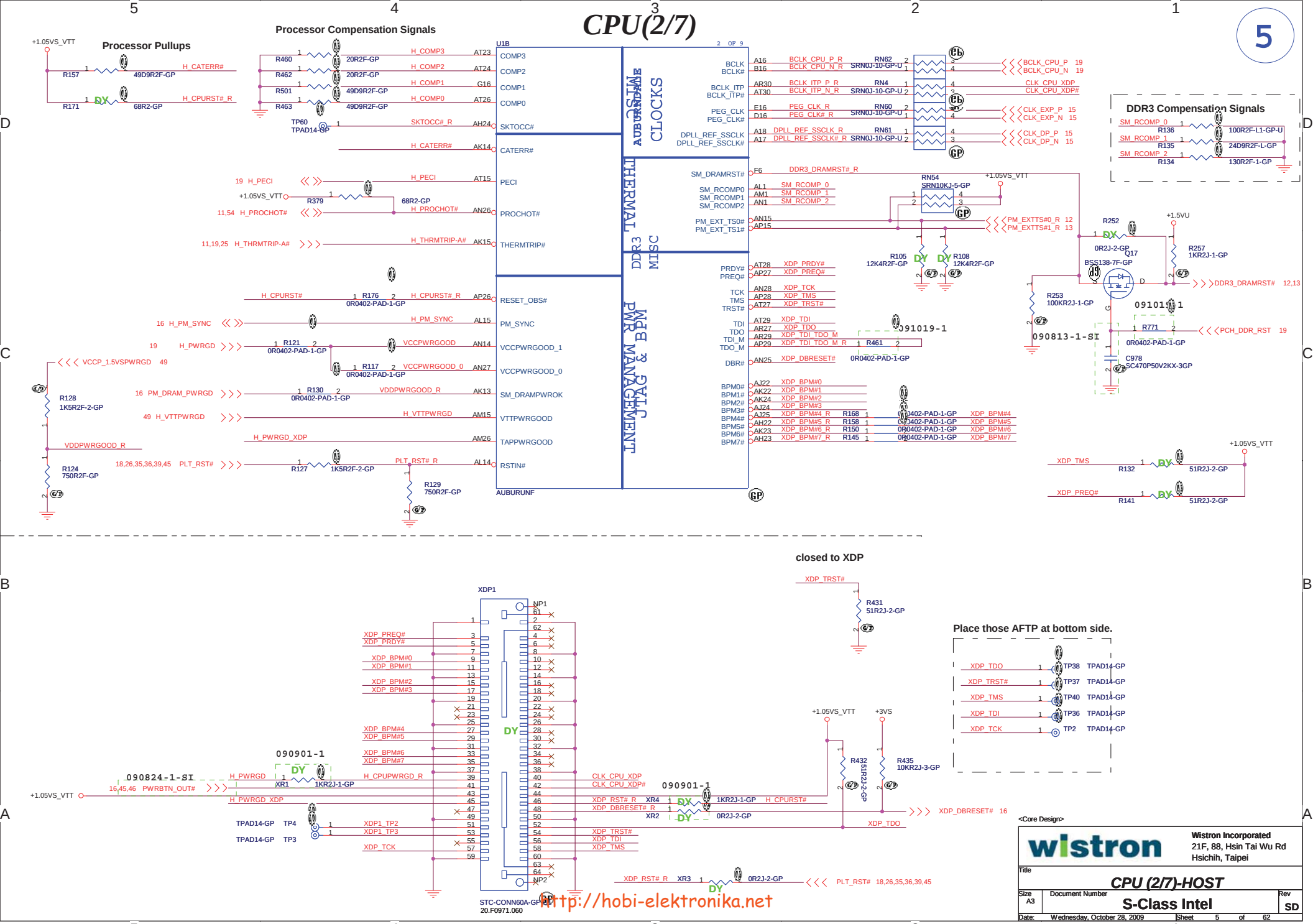
CPU(2/7)



<Core Design>

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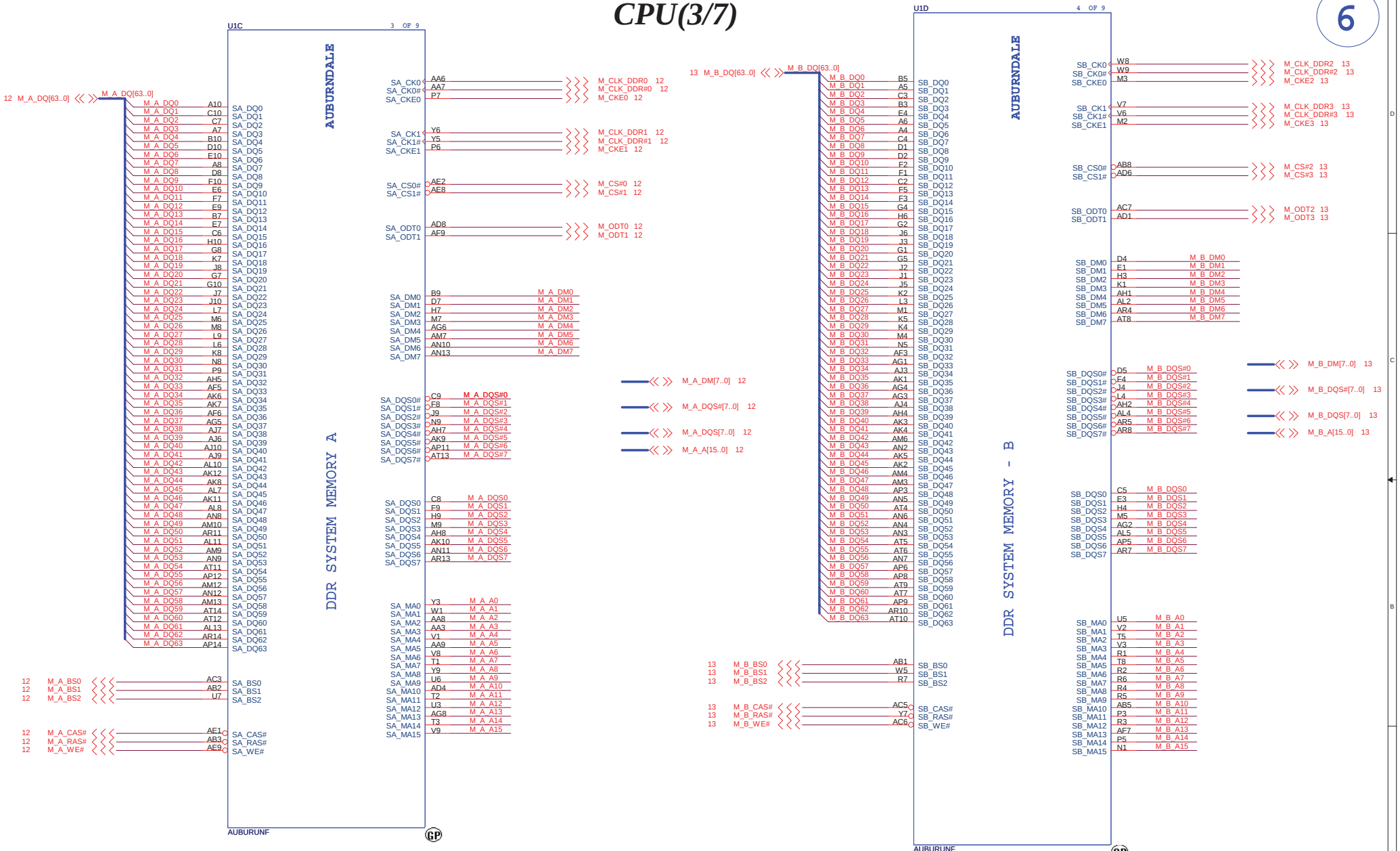
Title: CPU (2/7)-HOST

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 5 of 62

CPU(3/7)



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Title: CPU (3/7)-MEM INTERFACE

Size	Document Number	Rev
A3	S-Class Intel	SD

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CPU(4/7)

PROCESSOR CORE POWER
40A

+VCC_CORE

091015-1

C520 C504 C107 C531 C556 C553
C495 C539 C485 C118 C121 C110
C132 C98 C104 C131 C96 C92 C130 C563
C137 C133 C558 C557 C492 C500 C511 C90

SC10U6D3V5MX-3GP
SC22U6D3V5MX-2GP
DY

U1F
6 OF 9
AUBURUNF

AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

VTT0

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

AE10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

+1.05VS_VTT

C616 C491 C590 C555 C499 C135 C528 C93 C99
C115 C134 C119
C129 C108

SC22U6D3V5MX-2GP

+VTT_43 +VTT_44

R624 R700 0R0402-PAD-1-GP

091019-1

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail values are
Auburndale VTT=1.05V
Clarksfield VTT=1.1V

POWER

CPU VIDS

PSI# AN33 — PSI# 54

VID0 AK35 H_VID0
VID1 AK33 H_VID1
VID2 AK34 H_VID2
VID3 AL35 H_VID3
VID4 AL33 H_VID4
VID5 AM33 H_VID5
VID6 AM35 H_VID6

H_VID[6..0] 54

PROC_DPRSLPVR AM34 — PM_DPRSLPVR 54

VTT_SELECT G15 H_VTTVID1 — TP63 TPAD14-GP

H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

SENSE LINES

ISENSE AN35 — IMVP_IMON 54

091019-1

VCC_SENSE AJ34 VCC_SENSE_R
VSS_SENSE AJ35 VSS_SENSE_R

R178 R173 0R0402-PAD-1-GP

VCC_SENSE 54
VSS_SENSE 54

VTT_SENSE B15 VTT_SENSE
VSS_SENSE_VTT A15 VSS_SENSE_VTT

VTT_SENSE 58
VSS_SENSE_VTT 58

+VCC_CORE

R177 100R2F-L1-GP-U
R172 100R2F-L1-GP-U
R512 100R2F-L1-GP-U
R508 100R2F-L1-GP-U

VSS_SENSE_VTT
VTT_SENSE

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Title: CPU (4/7)-POWER
Size: Custom
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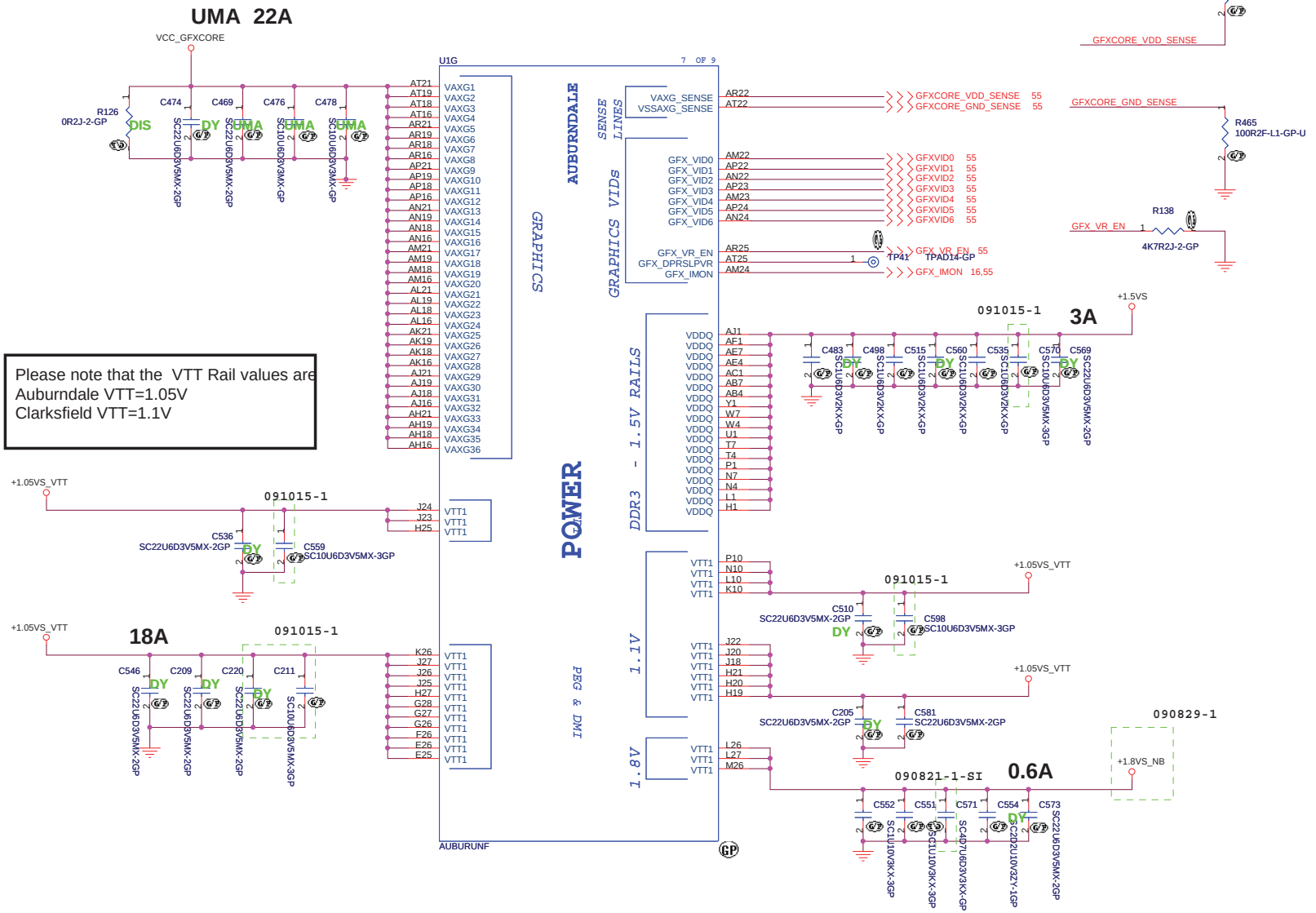
CPU(5/7)



<Core Design>

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Title: CPU (5/7)-Graphic POWER

Size: A3 | Document Number: S-Class Intel | Rev: SD

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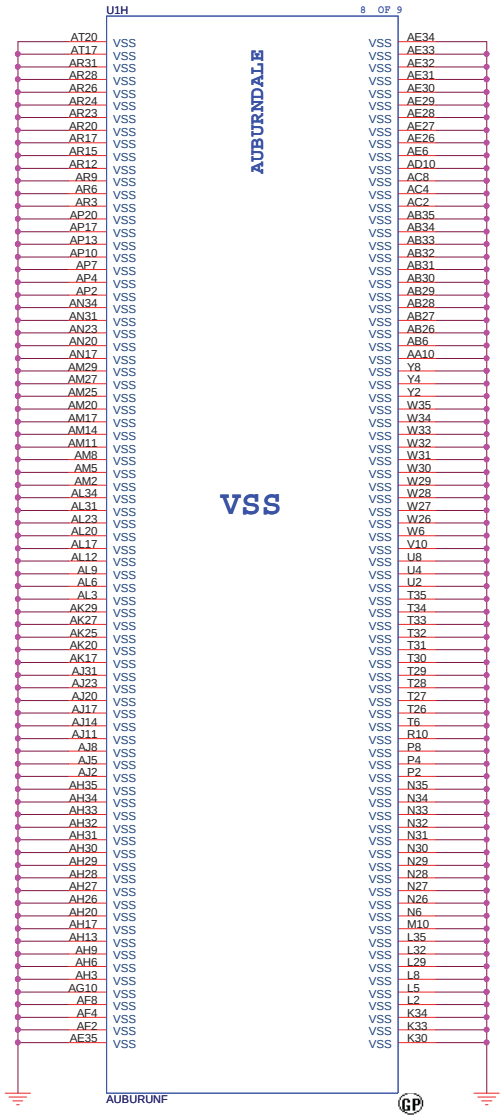
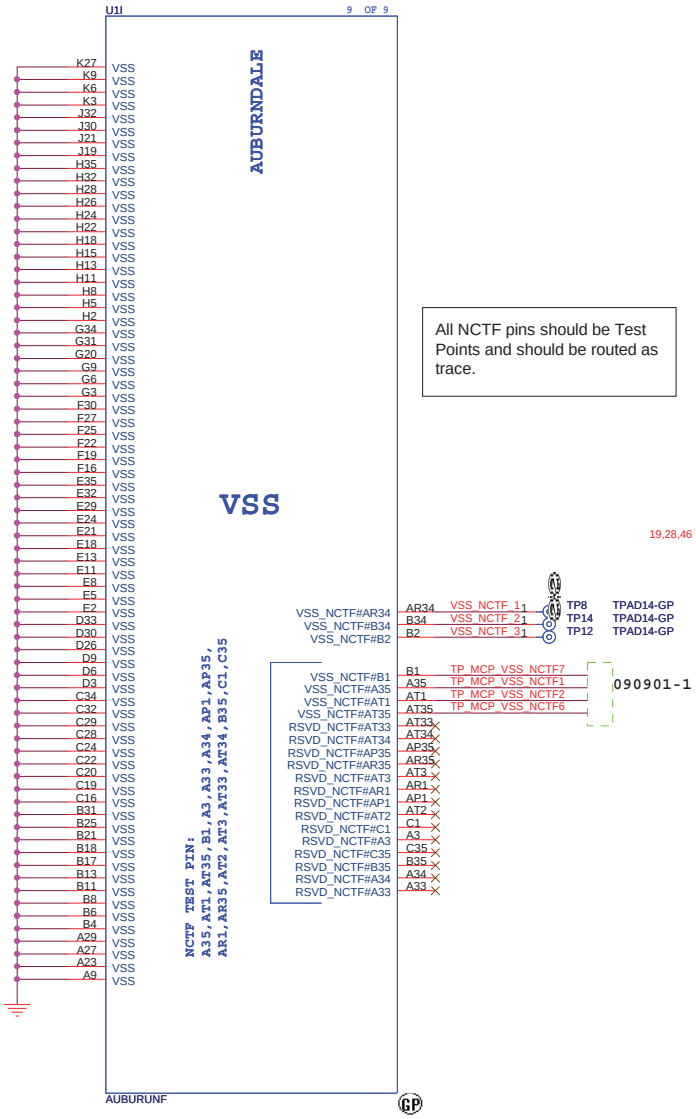
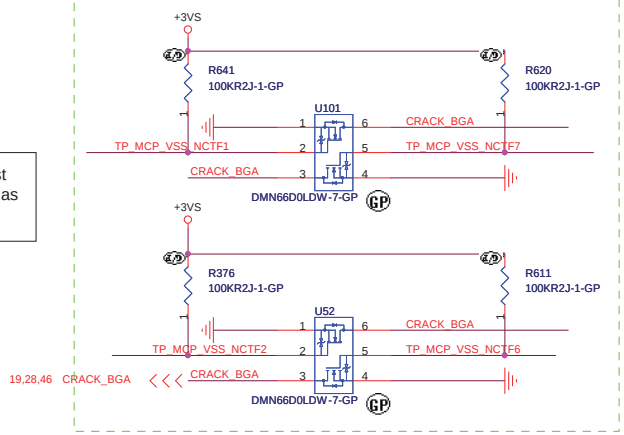
CPU(6/7)





All NCTF pins should be Test Points and should be routed as trace.

090829-1



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Title: CPU (6/7)-VSS

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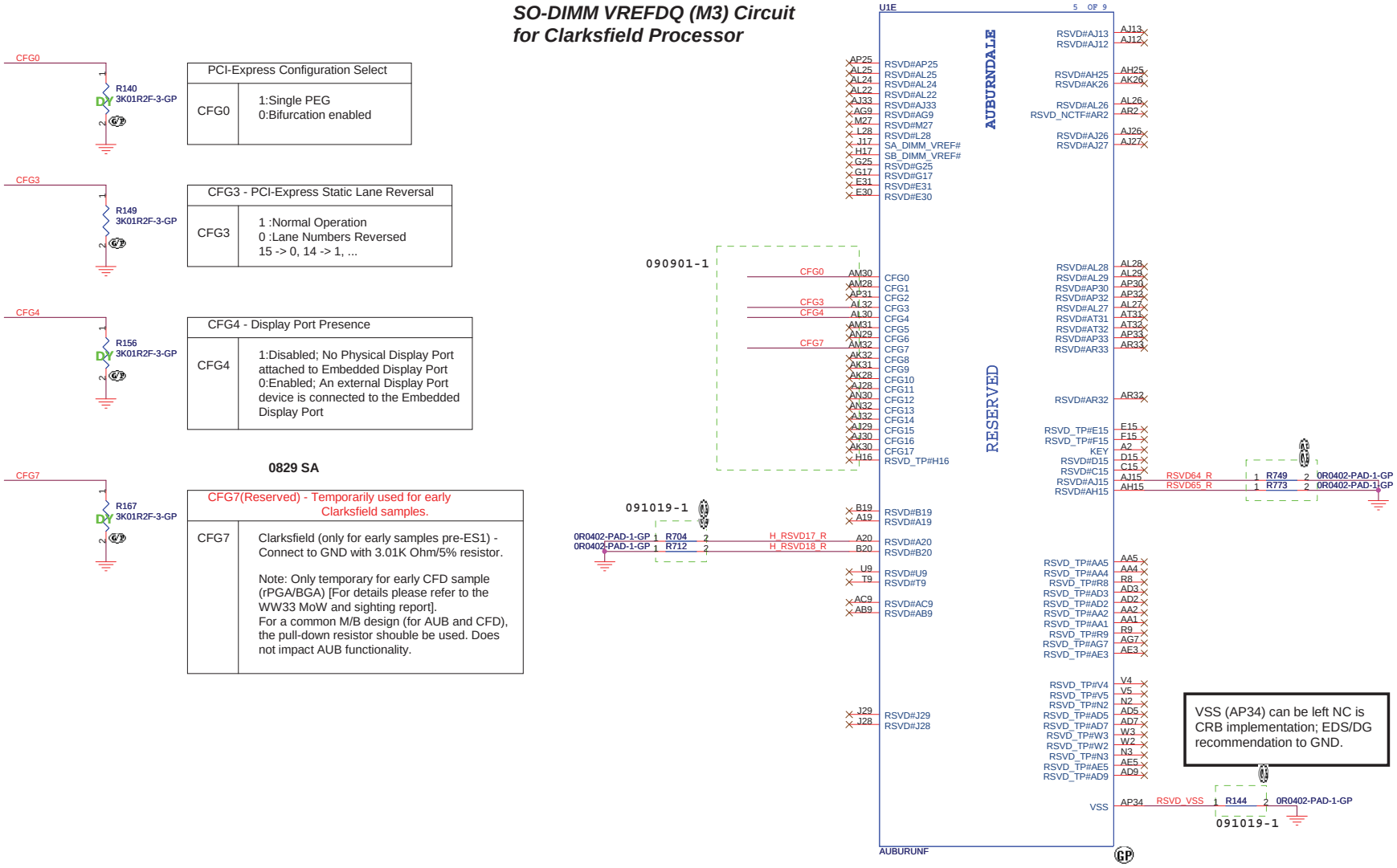
CPU(7/7)

SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor



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Title: CPU (7/7)-RESERVED

Size: A3 | Document Number: S-Class Intel | Rev: SD

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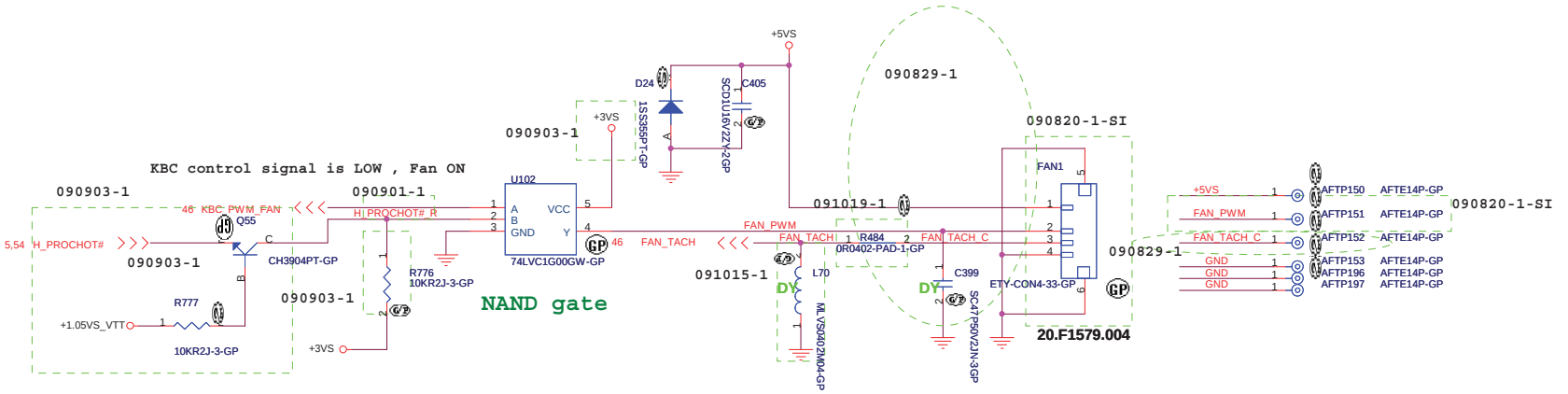
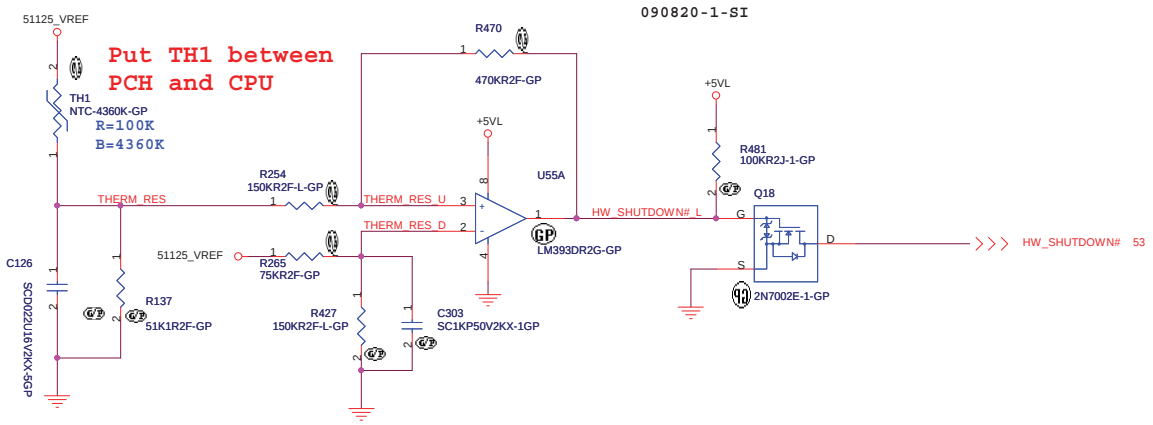
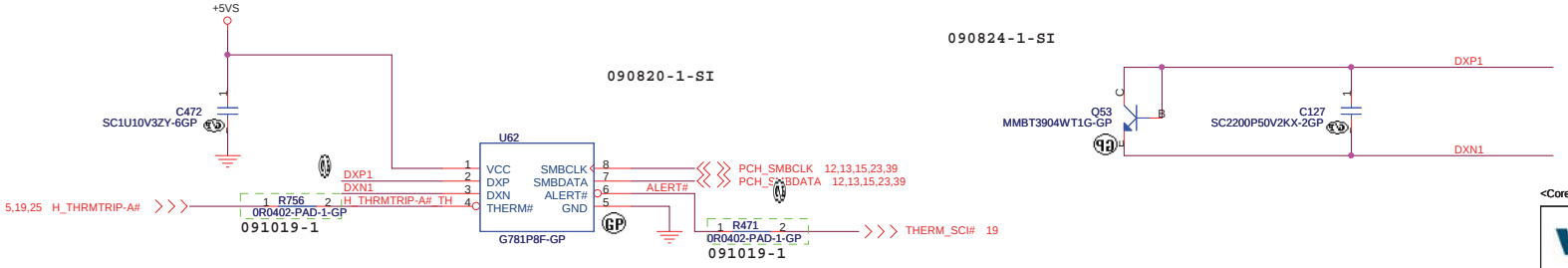
4 WIRE PWM Fan Control circuit



T8 H/W Shutdown Control circuit



Thermal IC Control circuit



http://hobi-elektronika.net

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Title: G787S11U-GP THERMAL

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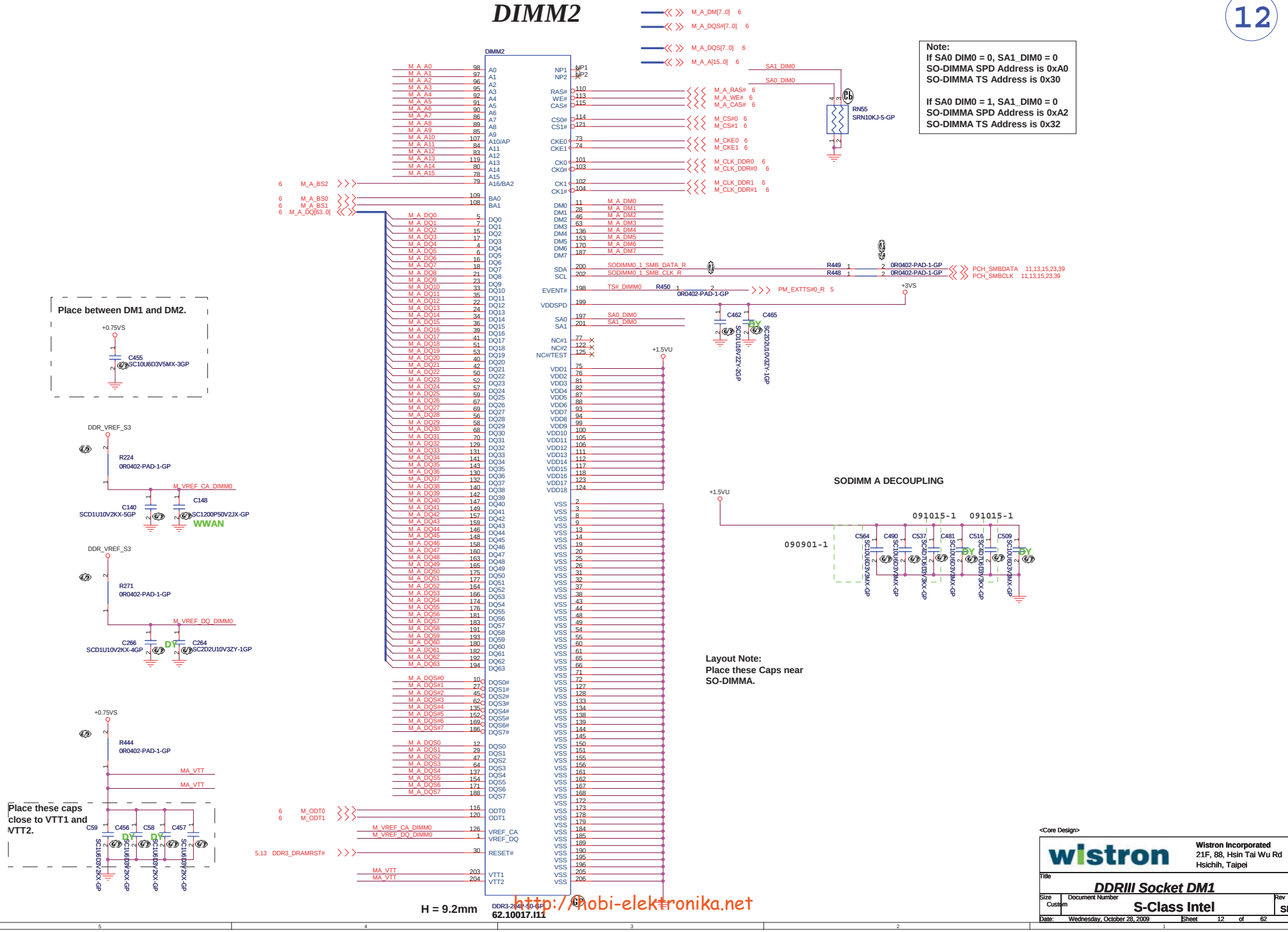
DIMM2



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Title: DDRIII Socket DM1

Size: Custom | Document Number: S-Class Intel | Rev: SD

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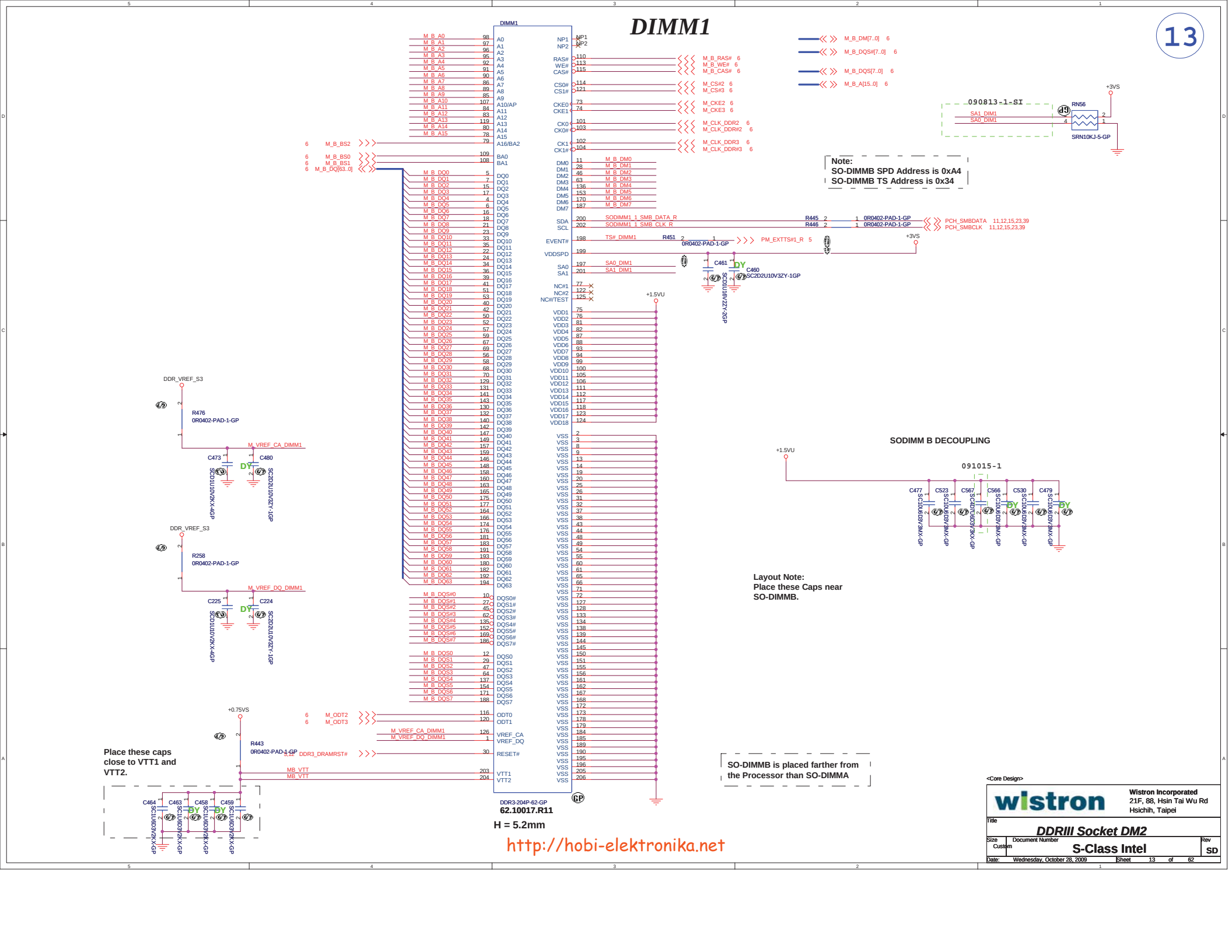
DIMM1



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Title: DDRIII Socket DM2

Size: Custom | Document Number: S-Class Intel | Rev: SD

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PCH(1/9)

14

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

U3A 1 OF 10

RTC: RTCX1 B13, RTCX2 D13, RTCRST# C14, SRTCRST# D17, INTRUDER# A16, INTVRMEN A14
LPC: FWH0/LAD0 D33, FWH1/LAD1 B33, FWH2/LAD2 C32, FWH3/LAD3 A32, FWH4/LFRAME# C34, LDRQ0# A34, LDRQ1#/GPIO23 F34, SERIRQ AB9
IHDA: HDA_BCLK A30, HDA_SYNC D29, SPKR P1, HDA_RST# C30, HDA_SDIN0 G30, HDA_SDIN1 F30, HDA_SDIN2 E32, HDA_SDIN3 F32, HDA_SDO B29
SATA: HDA_DOCK_EN#/GPIO33 H32, HDA_DOCK_RST#/GPIO13 J30; SATA0RXN AK7, SATA0RXP AK6, SATA0TXN AK11, SATA0TXP AK9; SATA1RXN AH6, SATA1RXP AH5, SATA1TXN AH9, SATA1TXP AH8; SATA2RXN AF11, SATA2RXP AF9, SATA2TXN AF7, SATA2TXP AF6; SATA3RXN AH3, SATA3RXP AH1, SATA3TXN AF3, SATA3TXP AF1; SATA4RXN AD9, SATA4RXP AD8, SATA4TXN AD6, SATA4TXP AD5; SATA5RXN AD3, SATA5RXP AD1, SATA5TXN AB3, SATA5TXP AB1; SATACOMPO AF16, SATACOMPI AF15
JTAG: JTAG_TCK M3, JTAG_TMS K3, JTAG_TDI K1, JTAG_TDO J2, TRST# J4
SPI: SPI_CLK BA2, SPI_CS0# AV3, SPI_CS1# AY3, SPI_MOSI AY1, SPI_MISO AV1; SATALED# T3, SATA0GP/GPIO21 Y9, SATA1GP/GPIO19 V1
IBEXPEAK-M-GP-NF

HDD: SATA0RXN/SATA0RXP/SATA0TXN/SATA0TXP → SATA_RXN0 35, SATA_RXP0 35, SATA_TXN0 35, SATA_TXP0 35
ODD: SATA1RXN/SATA1RXP/SATA1TXN/SATA1TXP → SATA_RXN1 35, SATA_RXP1 35, SATA_TXN1 35, SATA_TXP1 35
ESATA: SATA4RXN/SATA4RXP/SATA4TXN/SATA4TXP → SATA_RXN4 44, SATA_RXP4 44, SATA_TXN4 44, SATA_TXP4 44

LPC_AD[0..3] 45,46; LPC_FRAME# 45,46; SIRQ 45,46; PCH_GPIO23 → TP112 TPAD14-GP (090821-1-SI)

NO REBOOT STRAP

090829-1

R336 10KR2J-3-GP (DY) HDA_SPKR
R636 10KR2J-3-GP SIRQ

No Reboot Strap R336	
HDA_SPKR	Low = Default High = No Reboot

VTAP Assumed as 1.1V

PCH_JTAG_RST# R347 51R2F-2-GP (DY)
PCH_JTAG_TCK R338 4K7R2J-2-GP (DY)
PCH_JTAG_TMS R342 51R2F-2-GP (DY)
PCH_JTAG_TDO R351 51R2F-2-GP (DY)
PCH_JTAG_TDI R345 51R2F-2-GP (DY)
PCH_JTAG_RST# R349 10KR2J-3-GP

+1.05VS

Place the resistors on RST, TCK, TMS, and TDI near PCH.

Place the resistors on TDO near XDP.

090829-1: PCH_JTAG_TCK, PCH_JTAG_TMS, PCH_JTAG_TDI, PCH_JTAG_TDO, PCH_JTAG_RST#

091008-1: R295 33R2J-2-GP KBC_SPI_CLK_R; R296 100KR2J-1-GP; R303 0R0402-PAD-1-GP KBC_SPI_CS0#_R; R300 0R0402-PAD-1-GP KBC_SPI_CS1#_R; R297 33R2J-2-GP KBC_SPI_SI_R

090813-1-SI: 46 KBC_SPI_CLK, 46 KBC_SPI_CS0#, 46 KBC_SPI_CS1#, 46 KBC_SPI_SI, 46 KBC_SPI_SO

091019-1: R633 10KR2J-3-GP (+3VS); R326 0R0402-PAD-1-GP; SATA0GP; HDD_HALTLED 1 → HDD_HALTLED 34

090901-1: SATA_LED# → EC984 SC470P50V2KX-3GP; SATA_LED# 34

R634 37D4R2F-GP (SATACOMP, +1.05VS)

R323 10KR2J-3-GP (HDD_HALTLED, +3VS)

Oscillator

ICH_RTCX1 — R358 10MR2J-L-GP — ICH_RTCX2

090903-1: X1 X-32D768KHZ-38GPU 82.30001.691

090825-1-SI: C386 SC15P50V2JN-2-GP; C387 SC15P50V2JN-2-GP

32.768Khz 12.5pf 10ppm
1st: 82.30001.691 (KDS)

BIOS have Default code & Run code. If we want to flash default code area, we should set GPIO33 be Low when SYS_PWROK assert.

+3VS — R719 10KR2J-3-GP (DY) — GPIO33 — R692 1KR2F-3-GP — Q48 2N7002E-1-GP

46,51 WHITE_BATLED# — R718 0R2J-2-GP (DY)

RTC Battery

+RTCVCC — 091019- W=20mils — R352 0R0402-PAD-1-GP W=20mils — RTC_PWR_L — U43 CH715FPT-GP — RTC_PWR W=20mils — R353 1KR2J-1-GP — BATT1.1

090829-1: 3D3V_AUX_S5_5_51125

C372 SC1U10V3KX-3GP

090819-1-SI: RTC1 PWR GND NP1 NP2 — BAT-BH3201-C1401-7H-GP 62.70001.031

090829-1

<Core Design>

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Title: PCH (1/9)-SATA/SPI/LPC

Size	Document Number	Rev
A3	S-Class Intel	SD

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PCH(2/9)

U3B — 2 OF 10 — IBEXPEAK-M-GP-NF

PCI-E* / SMBus / Controller Link / PEG / From CLK BUFFER / Clock Flex

EXP
35 PCIE_RXN2 — SCD1U10V2KX-5GP — C321 TXN2 — BG30 PERN1
35 PCIE_RXP2 — SCD1U10V2KX-5GP — C320 TXP2 — BJ30 PERP1
35 PCIE_TXN2 — BF29 PETN1
35 PCIE_TXP2 — BH29 PETP1
AW30 PERN2
BA30 PERP2
BC30 PETN2
BD30 PETP2

WLAN
39 PCIE_RXN4 — SCD1U10V2KX-5GP — C326 TXN4 — AU30 PERN3
39 PCIE_RXP4 — SCD1U10V2KX-5GP — C327 TXP4 — AT30 PERP3
39 PCIE_TXN4 — AU32 PETN3
39 PCIE_TXP4 — AV32 PETP3
BA32 PERN4
BB32 PERP4
BD32 PETN4
BE32 PETP4

LAN
36 PCIE_RXN6 — SCD1U10V2KX-5GP — C768 TXN6 — BF33 PERN5
36 PCIE_RXP6 — SCD1U10V2KX-5GP — C765 TXP6 — BH33 PERP5
36 PCIE_TXN6 — BG32 PETN5
36 PCIE_TXP6 — BJ32 PETP5
BA34 PERN6
AW34 PERP6
BC34 PETN6
BD34 PETP6

AT34 PERN7
AU34 PERP7
AU36 PETN7
AV36 PETP7
BG34 PERN8
BJ34 PERP8
BG36 PETN8
BJ36 PETP8

SMBALERT#/GPIO11 — B9 — D32 CH751H-40-1-GP — LID_SW# 32,45,46
SMBCLK — H14 — PCH_SMB_CLK
SMBDATA — C8 — PCH_SMB_DATA
SML0ALERT#/GPIO60 — J14 — PCH_UPEK_INIT#
SML0CLK — C6 — SML0_CLK
SML0DATA — G8 — SML0_DATA
SML1ALERT#/GPIO74 — M14 — LPD_SPI_INTR#
SML1CLK/GPIO58 — E10 — SML1CLK
SML1DATA/GPIO75 — G12 — SML1DAT
090820-1-SI

CL_CLK1 — T13
CL_DATA1 — T11
CL_RST1# — T9

PEG_A_CLKRQ#/GPIO47 — H1 — PEG_CLKREQ#
CLKOUT_PEG_A_N — AD43 — CLK_PCH_PEGA_N — R792 0R0402-PAD-1-GP — CLK_PCIE_VGA# 24
CLKOUT_PEG_A_P — AD45 — CLK_PCH_PEGA_P — R793 0R0402-PAD-1-GP — CLK_PCIE_VGA 24
CLKOUT_DMI_N — AN4 — CLK_EXP_N — CLK_EXP_N 5
CLKOUT_DMI_P — AN2 — CLK_EXP_P — CLK_EXP_P 5
091019-1

CLKOUT_DP_N/CLKOUT_BCLK1_N — AT1 — CLK_DP_N — CLK_DP_N 5
CLKOUT_DP_P/CLKOUT_BCLK1_P — AT3 — CLK_DP_P — CLK_DP_P 5
CLKIN_DMI_N — AW24 — CLK_CPU_DMI# — CLK_CPU_DMI# 23
CLKIN_DMI_P — BA24 — CLK_CPU_DMI — CLK_CPU_DMI 23
CLKIN_BCLK_N — AP3 — CLK_CPU_BCLK# — CLK_CPU_BCLK# 23
CLKIN_BCLK_P — AP1 — CLK_CPU_BCLK — CLK_CPU_BCLK 23
CLKIN_DOT_96N — F18 — DREFCLK# — DREFCLK# 23
CLKIN_DOT_96P — E18 — DREFCLK — DREFCLK 23
CLKIN_SATA_N/CKSSCD_N — AH13 — CLK_PCIE_SATA# — CLK_PCIE_SATA# 23
CLKIN_SATA_P/CKSSCD_P — AH12 — CLK_PCIE_SATA — CLK_PCIE_SATA 23
REFCLK14IN — P41 — CLK_ICH14 — CLK_ICH14 23
CLKIN_PCILOOPBACK — J42 — CLK_PCI_FB — CLK_PCI_FB 18

XTAL25_IN — AH51 — XTAL25_IN
XTAL25_OUT — AH53 — XTAL25_OUT
XCLK_RCOMP — AF38 — XCLK_RCOMP — R681 90D9R2F-1-GP — +1.05VS 25,46 SML1CLK_KBC

CLKOUTFLEX0/GPIO64 — T45 — CLK_PCI_SIO_DOCK — TP97 TPAD14-GP
CLKOUTFLEX1/GPIO65 — P43 — CLK_PCI_LPC — TP105 TPAD14-GP
CLKOUTFLEX2/GPIO66 — T42 — CLK_PCH_REF14 — TP98 TPAD14-GP
CLKOUTFLEX3/GPIO67 — N50 — CLK48_GPIO — R672 22R2J-2-GP — CLK48_5158 — CLK48_5158 38
C844 SC33P50V2JN-3GP

CLKOUT_PCIE0N — AK48
CLKOUT_PCIE0P — AK47
PCIECLKREQ0# — P9 — PCIECLKRQ0#/GPIO73
CLKOUT_PCIE1N — AM43
CLKOUT_PCIE1P — AM45
PCIECLKRQ1#/GPIO18 — U4 — PCIECLKREQ1# — R649 10KR2J-3-GP — +3VS
CLKOUT_PCIE2N — AM47 — CLK_PCIE_NEW# 35 — R774 0R0402-PAD-1-GP — CLK_PCIE_NEW#_R
CLKOUT_PCIE2P — AM48 — CLK_PCIE_NEW 35 — R789 0R0402-PAD-1-GP — CLK_PCIE_NEW_R
PCIECLKRQ2#/GPIO20 — N4 — NEWCARD_CLKREQ# 35 — R689 0R0402-PAD-1-GP — NEWCARD_CLKREQ#_R — R346 10KR2J-3-GP — +3VS
091019-1
CLKOUT_PCIE3N — AH42
CLKOUT_PCIE3P — AH41
PCIECLKRQ3#/GPIO25 — A8 — PCIECLKREQ3#
CLKOUT_PCIE4N — AM51 — CLK_PCIE_MINI_2#_R — R790 0R0402-PAD-1-GP — CLK_PCIE_MINI2# 39
CLKOUT_PCIE4P — AM53 — CLK_PCIE_MINI_2_R — R791 0R0402-PAD-1-GP — CLK_PCIE_MINI2 39
PCIECLKRQ4#/GPIO26 — M9 — CLKREQ_WLAN# — CLKREQ_WLAN# 39 — RN88 SRN10KJ-5-GP — +3VALW
CLKOUT_PCIE5N — AJ50
CLKOUT_PCIE5P — AJ52
PCIECLKRQ5#/GPIO44 — H6 — PCIECLKREQ5#
CLKOUT_PEG_B_N — AK53
CLKOUT_PEG_B_P — AK51
PEG_B_CLKRQ#/GPIO56 — P13 — PEG_B_CLKREQ#

RN80 SRN10KJ-5-GP — +3VALW — PEG_B_CLKREQ# — CLKREQ_WLAN# — PCIECLKREQ0#

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).

CLKOUTFLEX3/GPIO67: Configurable as an programmable output clock 48MHz output to SIO.

090915-1 — R764 10KR2J-3-GP — +3VALW
090829-1
090901-1
090903-1
091015-1
090820-1-SI
090818-1-SI
090824-1-SI
090825-1-SI

RN85 SRN2K2J-2-GP — SML0_CLK — PCH_SMB_CLK — SML0_DATA — PCH_SMB_DATA
RN53 SRN2K2J-1-GP — SML1DAT — SML1CLK
RN89 SRN10KJ-5-GP — PCH_UPEK_INIT# — LPD_SPI_INTR#
RN52 SRN2K2J-1-GP
RN92 SRN2K2J-1-GP
U47 DMN66D0LDW-7-GP — 11,12,13,23,39 PCH_SMBDATA — PCH_SMB_DATA — PCH_SMB_CLK — PCH_SMBCLK 11,12,13,23,39
U99 DMN66D0LDW-7-GP — SML1DAT — SML1DAT_KBC 25,46 — SML1CLK
C901 C388 C385 C383 SC33P50V2JN-3GP
SC820P50V3KX-GP
RN — +3VS — +3VALW — +3VL

C795 SC12P50V2JN-3GP — XTAL25_IN — UMA
X3 XTAL-25MHZ-113-GP — UMA
C807 SC12P50V2JN-3GP — XTAL25_OUT — UMA
R761 1MR2J-1-GP — UMA
R355 10KR2J-3-GP — PEG_CLKREQ#

<Core Design>

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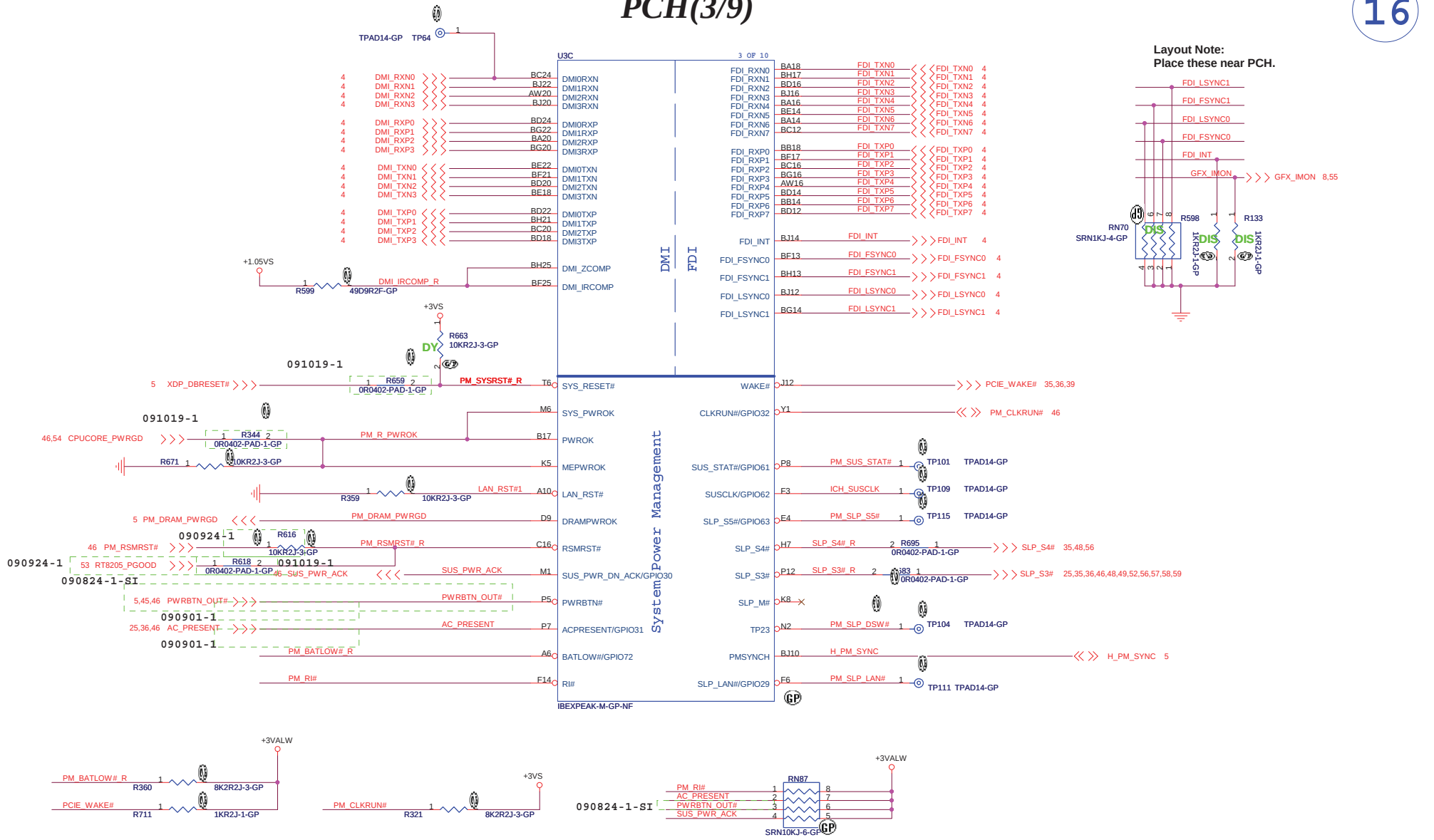
Title: PCH (2/9)-PCIE/SMBUS
Size: A3 | Document Number: S-Class Intel | Rev: SD
Date: Wednesday, October 28, 2009 | Sheet 15 of 62

PCH(3/9)



Layout Note:
Place these near PCH.

<Core Design>

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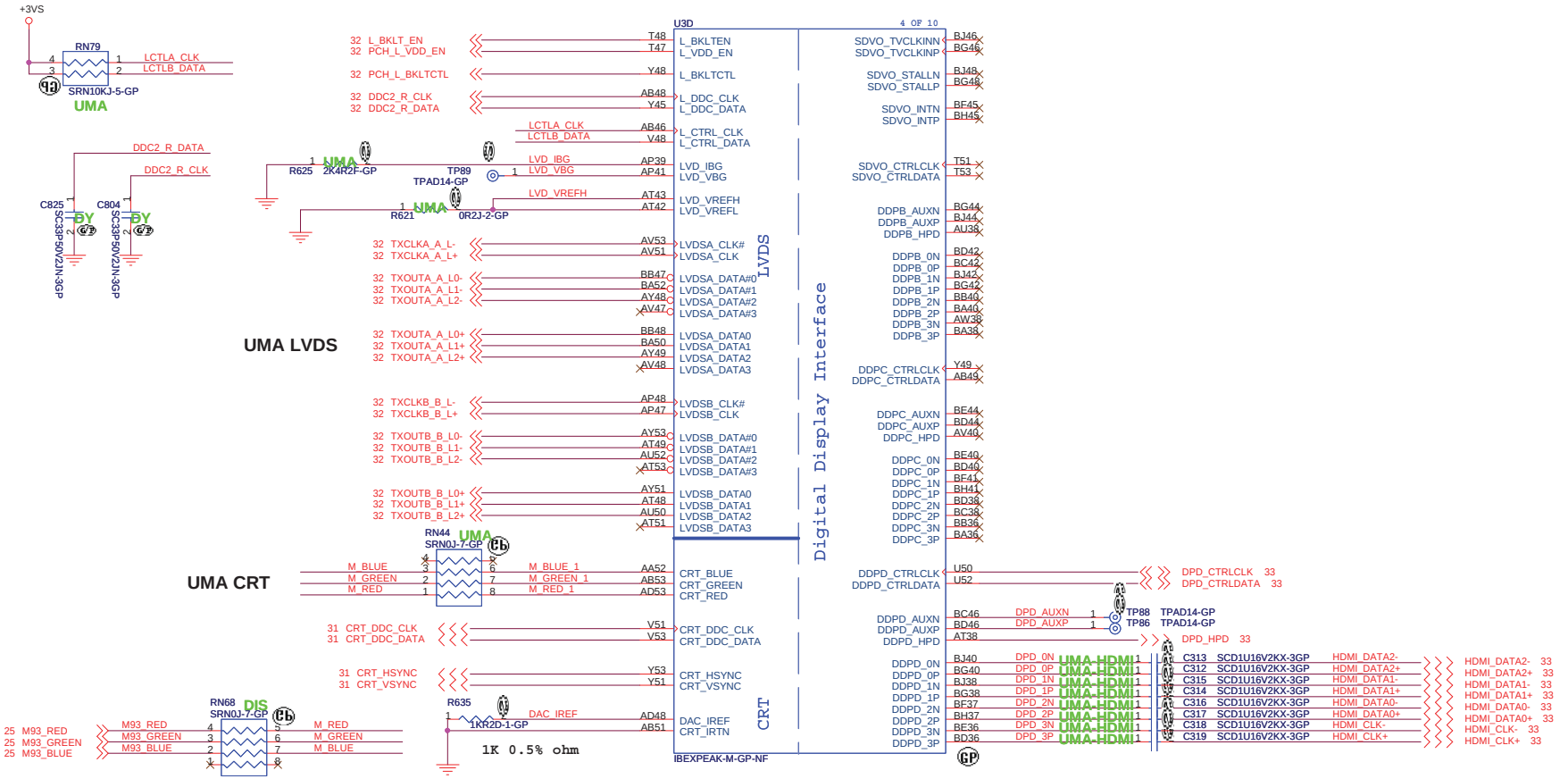
Title: PCH (3/9)-DMI/SYS PWR

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 16 of 62

PCH(4/9)



<Core Design>

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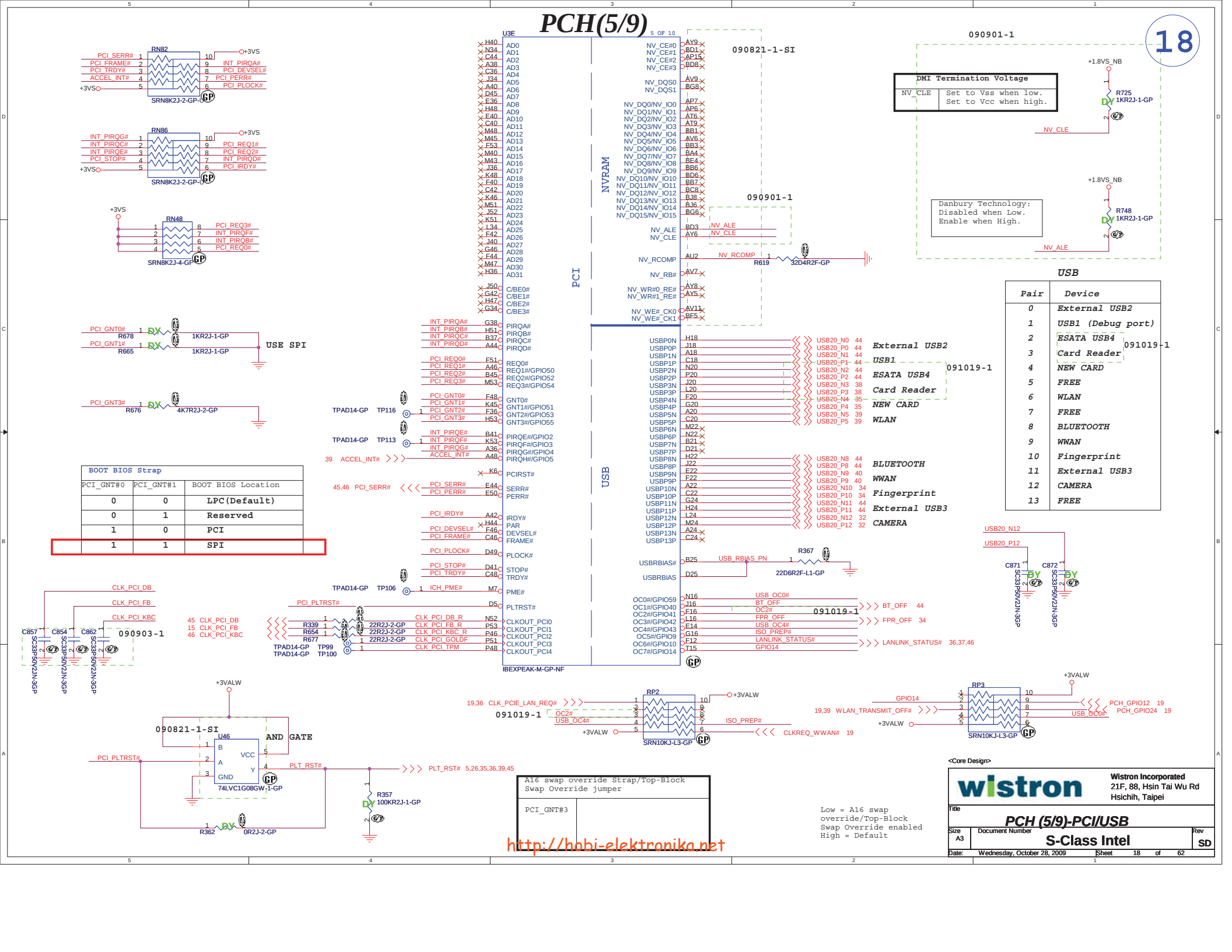
Title: PCH (4/9)-LVDS/CRT

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 17 of 62

PCH(5/9)



<Core Design>
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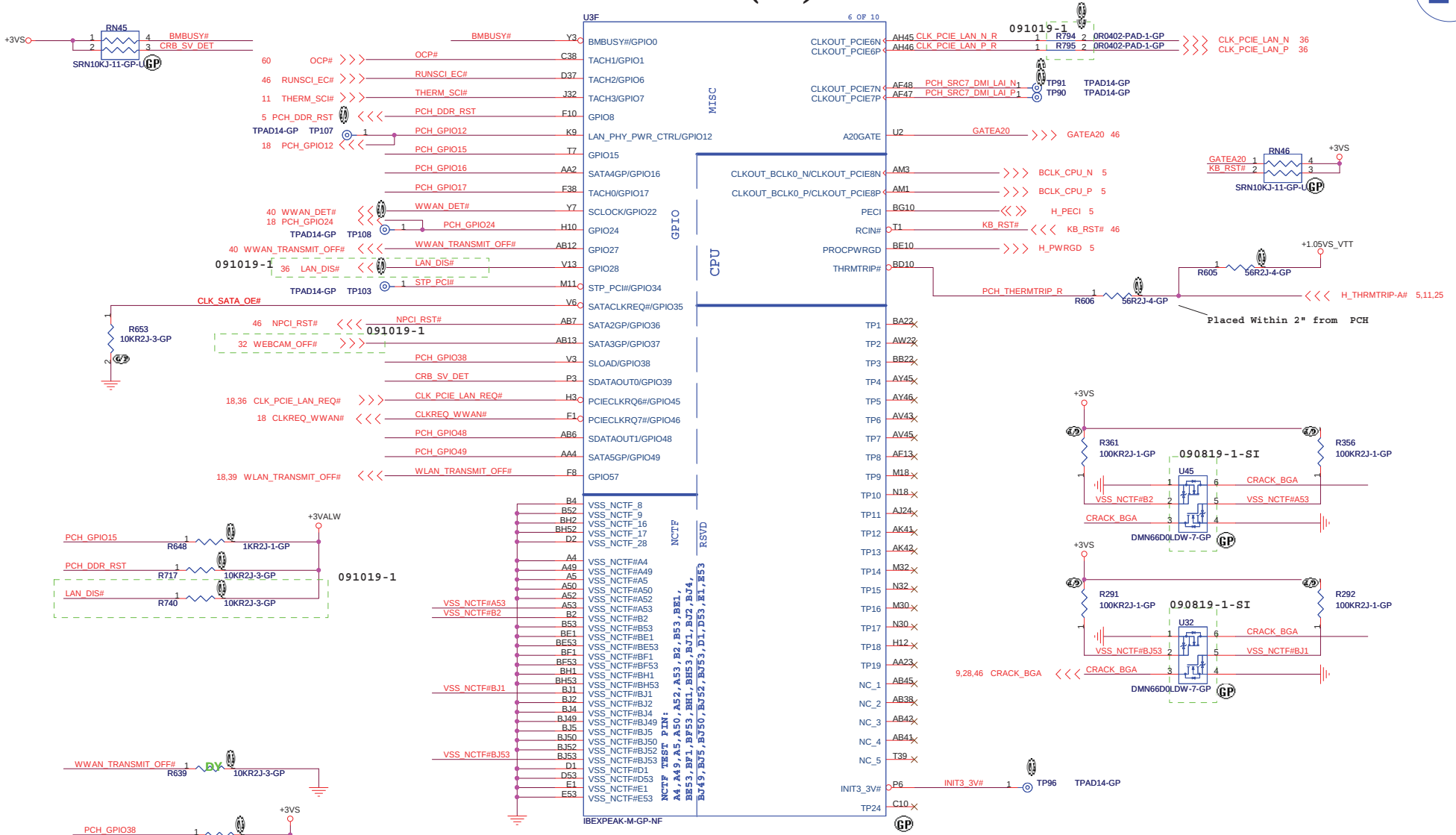
Hsichih, Taipei

Title: PCH (5/9)-PCI/USB

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 18 of 62

PCH(6/9)



<Core Design>

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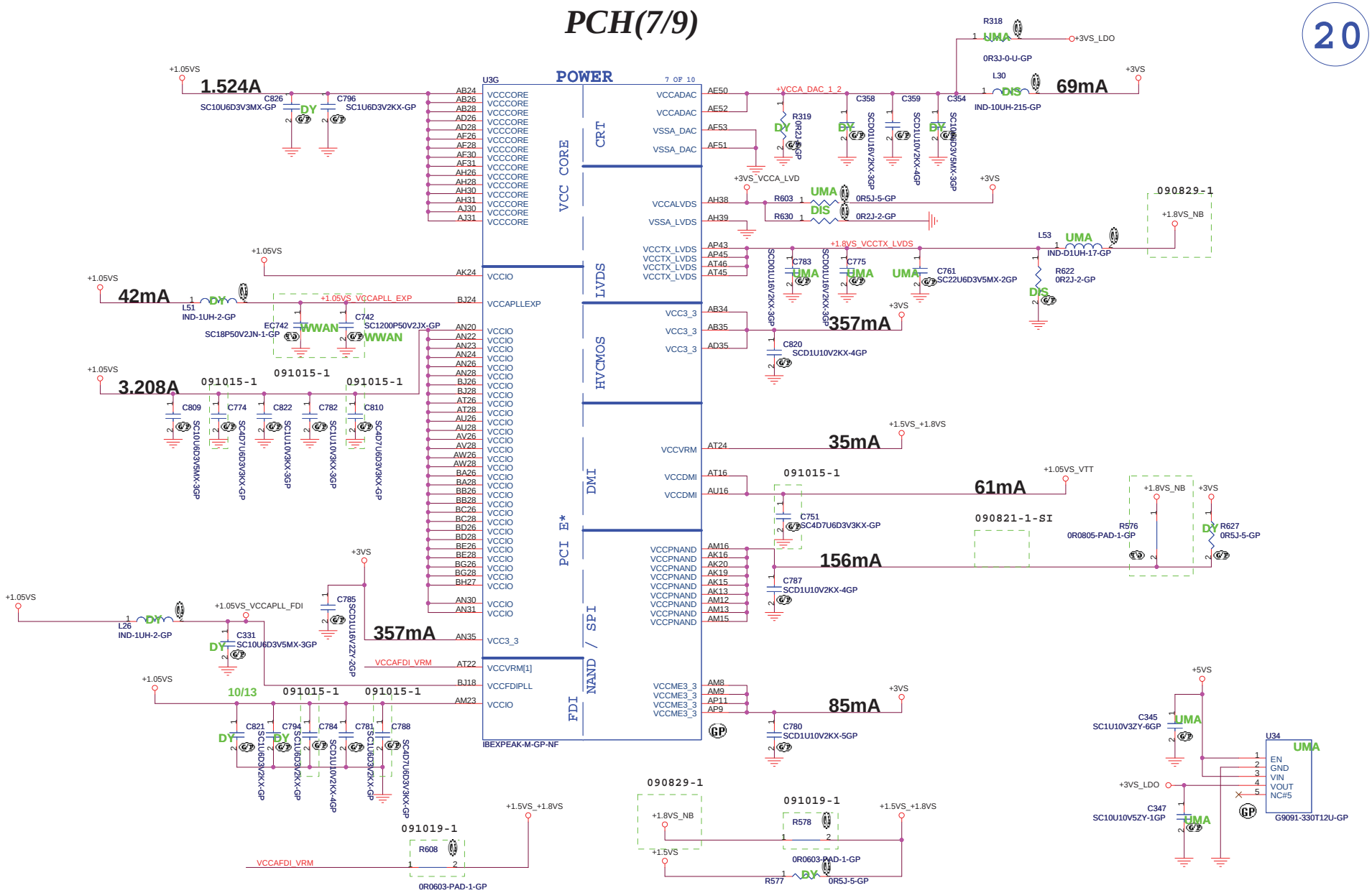
Title: PCH (6/9)-GPIO

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 19 of 62

PCH(7/9)



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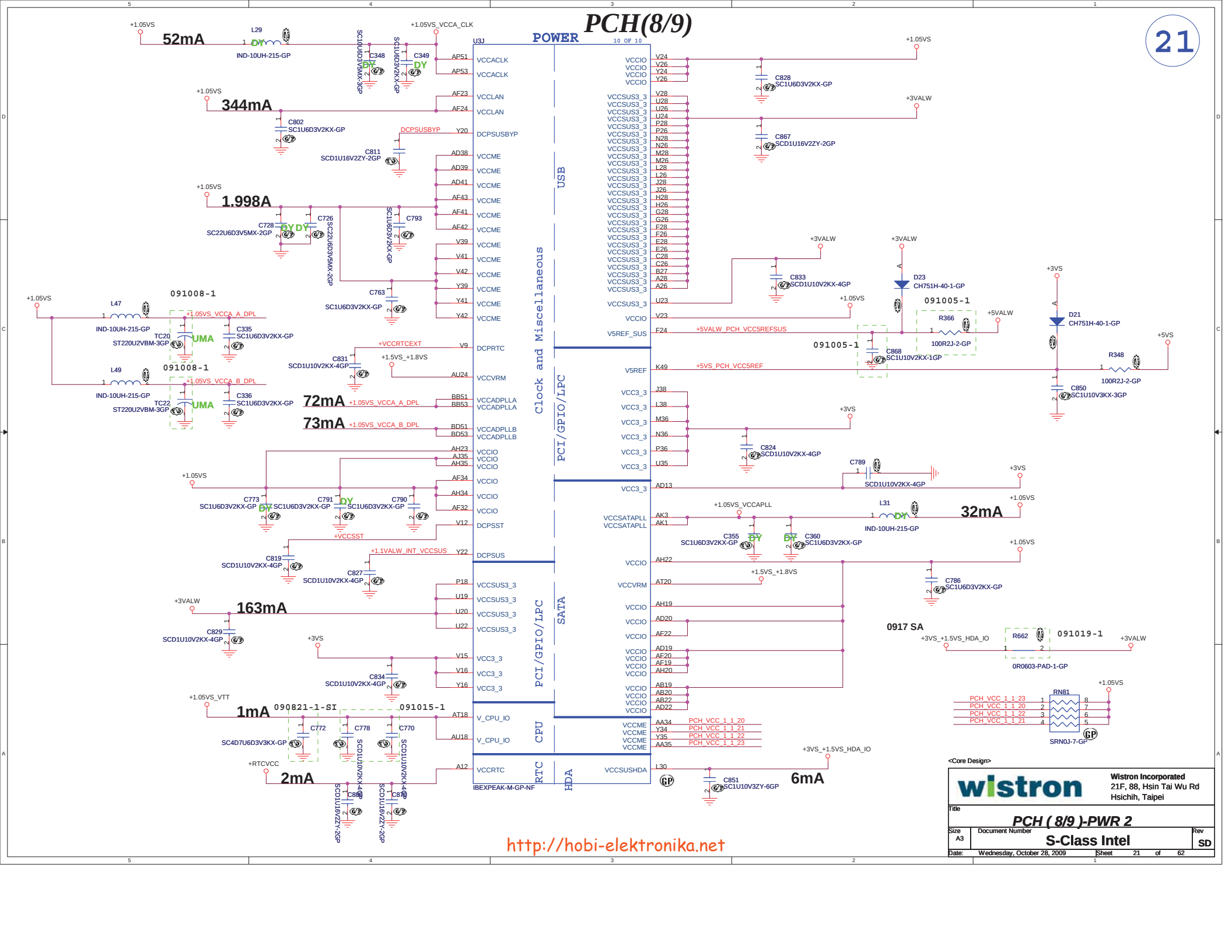
Title: PCH (7/9)-PWR 1		
Size: A3	Document Number: S-Class Intel	Rev: SD
Date: Wednesday, October 28, 2009	Sheet 20 of 62	

PCH(8/9)



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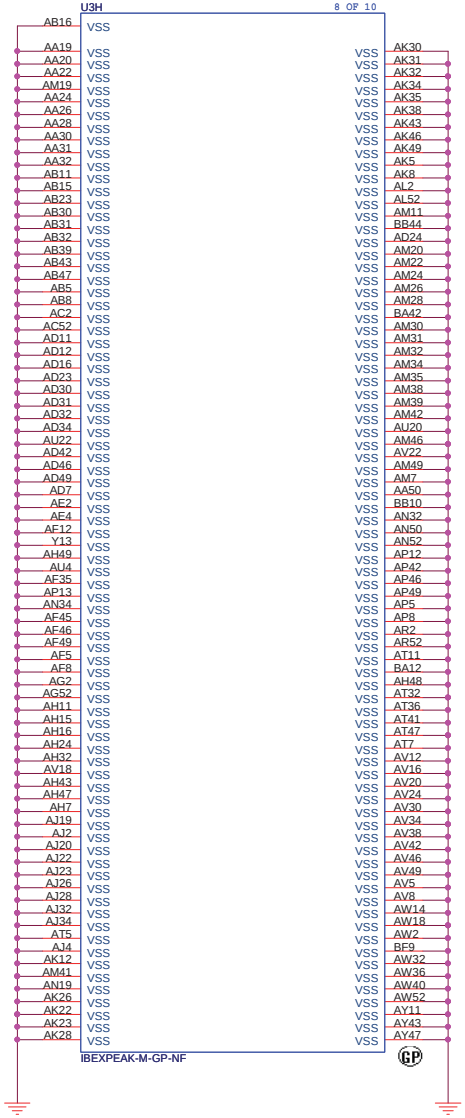
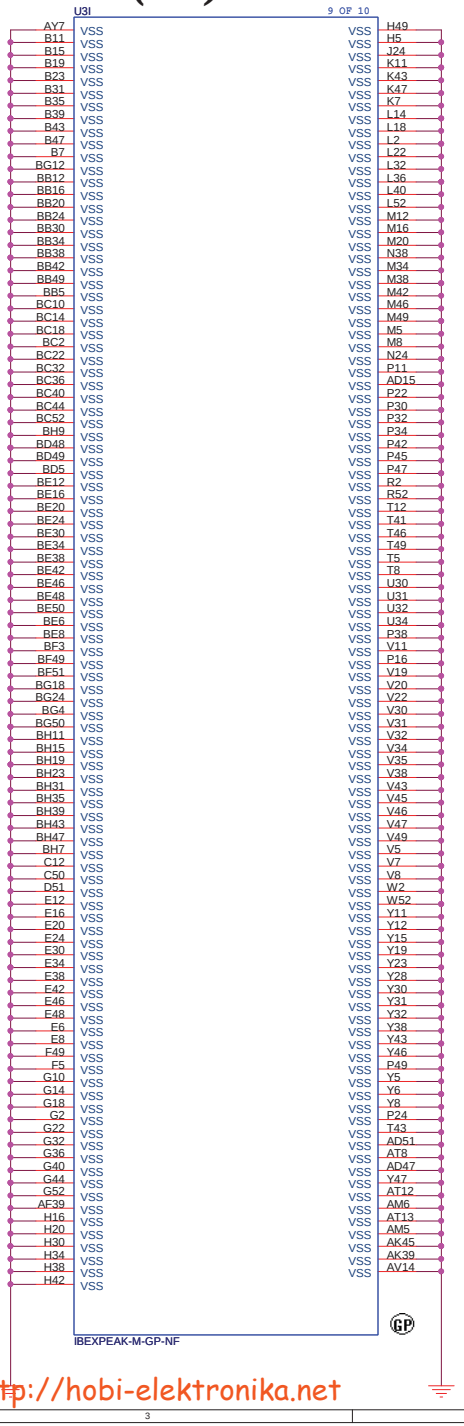
Title: PCH (8/9)-PWR 2

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 21 of 62

PCH(9/9)





<Core Design>

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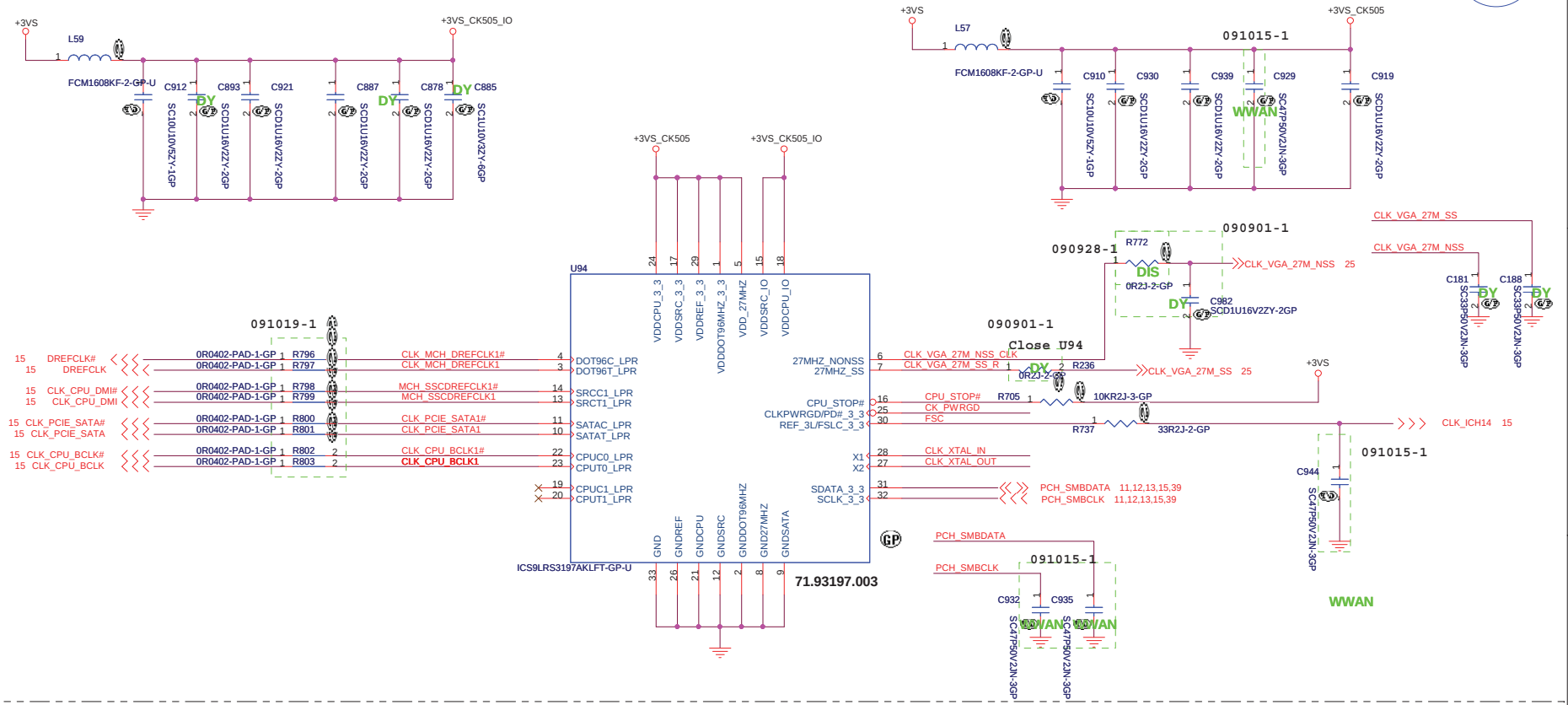
Title: PCH (9/9)-VSS

Size	Document Number	Rev
A3	S-Class Intel	SD

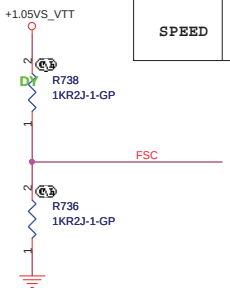
Date: Wednesday, October 28, 2009 Sheet 22 of 62

CLOCK GENERATOR

23

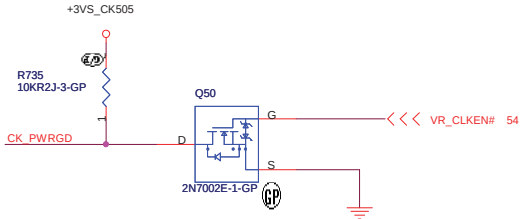


FSB Frequency Select

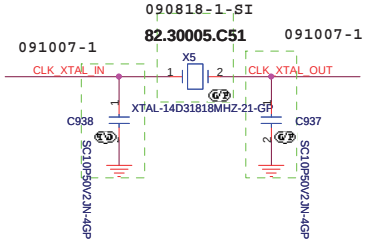


FSC	0	1
SPEED	133MHz (Default)	100MHz

Clock Gen. Eable



Clock Gen. Crystal



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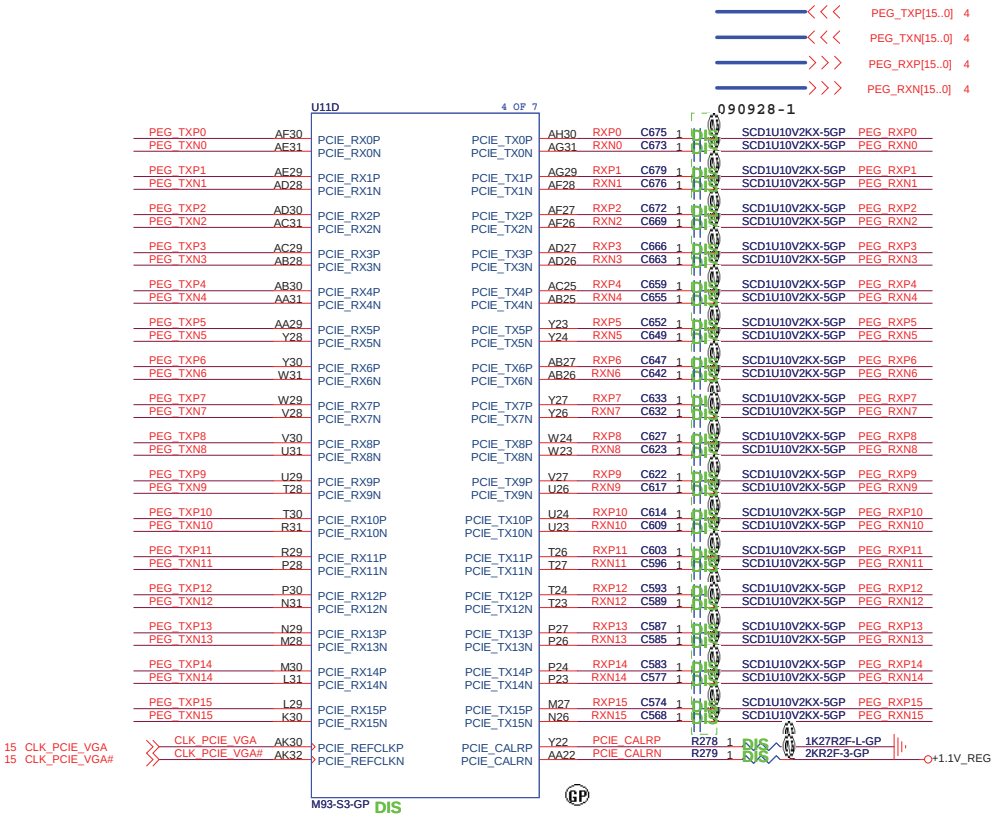
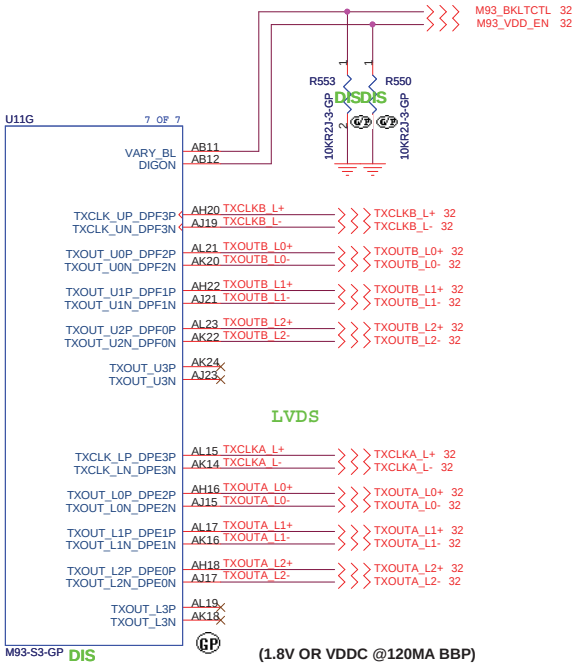
Title: Clock Generator ICS9LRS3197

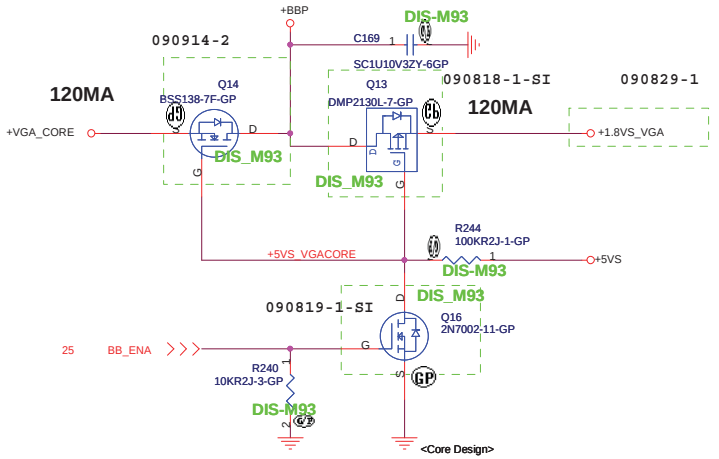
Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 Sheet 23 of 62

M93 GPU(1/5)







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Title: VGA-PCIE/LVDS(1/5)

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 24 of 62

M93 GPU(2/5)

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

0 = DON'T INSTALL RES
1 = INSTALL 10K RES
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M93-S3
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD BIF_VGA DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROM ID CFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 XX

090824-1-SI

VRAM ID:
BIT0 --> L:Quanta ; H:Wistron
BIT1 --> L:512M ; H:1GB
BIT2 --> L:Samsung ; H:Hynix
BIT3 -->N/A

090829-1

VRAM ID

090824-1-SI

M93 LP: VDDC=0.9/1.1V

Aperture Conig. PIN	M93S3 GPIO	Strapping Resistor	64MB VRAM	128MB VRAM	256MB VRAM
CONFIG0	GPIO_11	R243	0	0	1
CONFIG1	GPIO_12	R246	1	0	0
CONFIG2	GPIO_13	R250	0	0	0

GPIO20_VID1	GPIO15_VID0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

VRID 3210	Vendor	Type	Vendor P/N
0000	Hynix Orion-die	64*16-800MHZ	H5TQ1G63BFR-12C
0001	Samsung E-die	64*16-800MHZ	K4W1G1646E-HC12

LVDS

091019-1

091008-1

090820-1-SI

090903-1

090829-1

090818-1-SI

090819-1-SI

090824-1-SI

U11E

M93-S3-GP

HDMI

CRT

(1.8V @ 120MA DPLL_PVDD)
470R_1000mA
DPLL_PVSS

(1.1V @300MA DPLL_VDDC)
470R_1000mA
DPLL_PVSS

(1.8V @20MA TSVDD)
TSVSS

(1.8V @ 70MA AVDD)

(1.8V @ 45MA VDD1DI)

(1.8V @ 2MA A2VDDQ)

(3.3V @ 65MA A2VDD)

DO NOT INSTALL for M93-S3
Only for PARK-S3

VOLTAGE DIVIDER TO MAKE XTALIN VOLTAGE LEVEL OF 1.8V

VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = .6V)

Optional RC network to fine tune PWR SEQ.

<Core Design>

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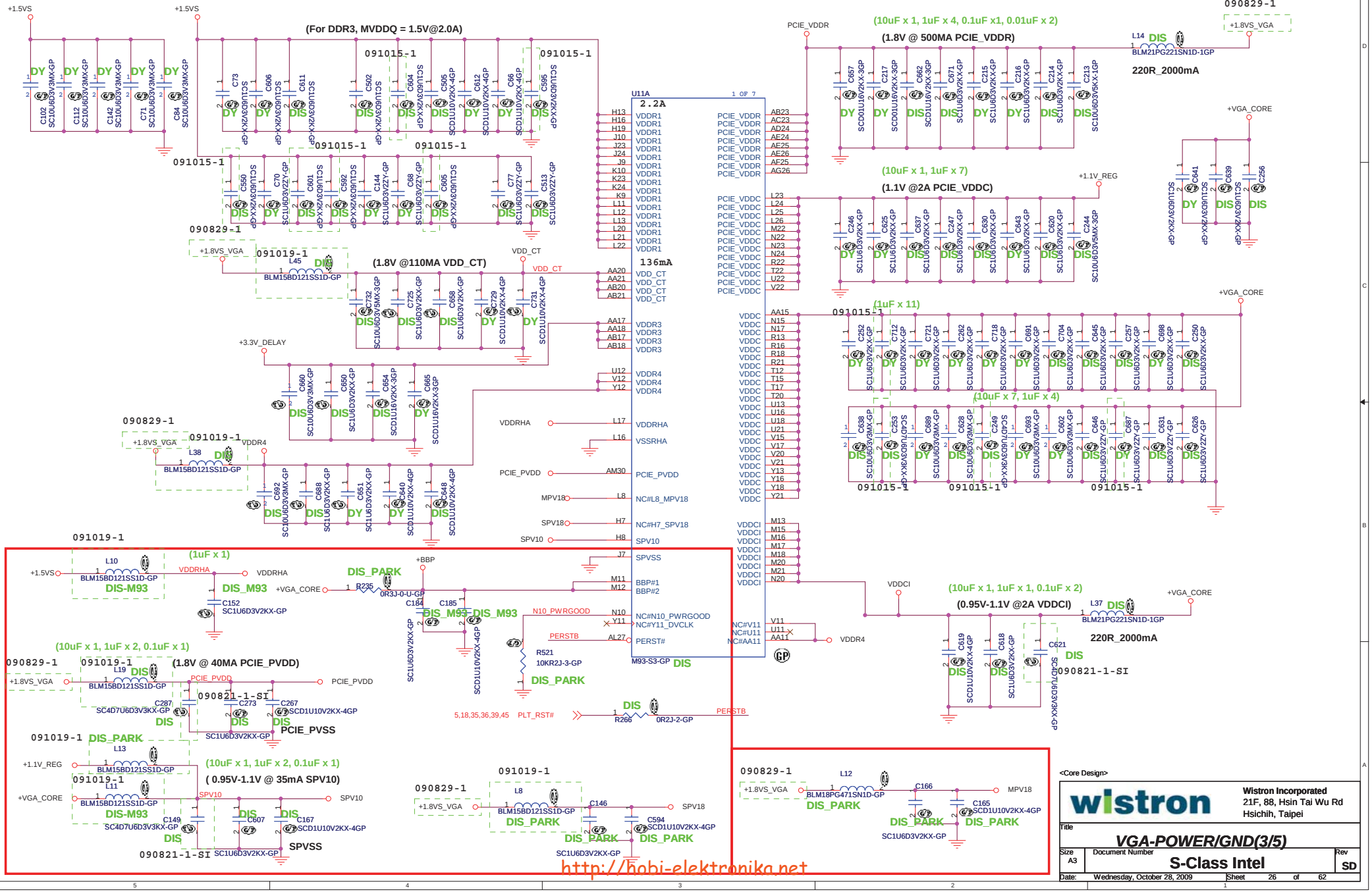
Title: LCD/CRT/HDMI PORT(2/5)

Size: A2 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 25 of 62

M93 GPU(3/5)



<Core Design>

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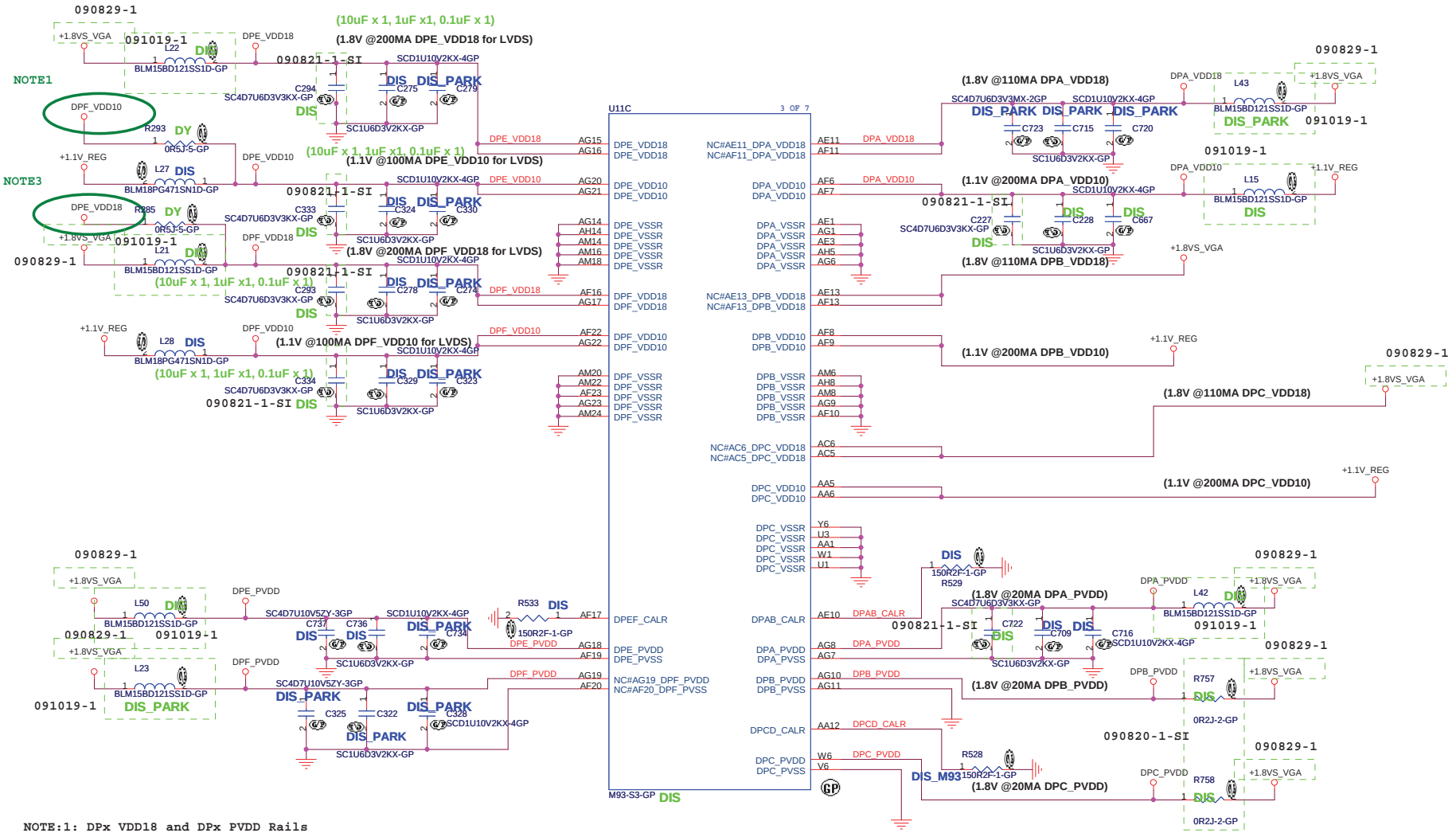
Hsichih, Taipei

Title: VGA-POWER/GND(3/5)

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 26 of 62

M93 GPU(4/5)



NOTE:1: DPx_VDD18 and DPx_PVDD Rails can be join together and remove Decoupling Capacitors and BEAD for DPx_PVDD if signal integrity for DP lanes are OK.

NOTE:2: DPA_VDD10 / DPB_VDD10 and DPE_VDD10 / DPF_VDD10 Rails can be join together and remove Decoupling Capacitors and BEADfor one rail of each pair if signal integrity for DP lanes are OK.
We also need to Change BEAD to minimum 400mA rating.

NOTE:3: DPx_VDD18 Rails can be join together as shown in schematic for Dual -Link DVI or LVDS setting and remove DecouplingCapacitors and BEAD of any one rail of the pair if signal integrity for DP lanes are OK.
We need at least 500mA Bead to supportjoin rails.

<Core Design>

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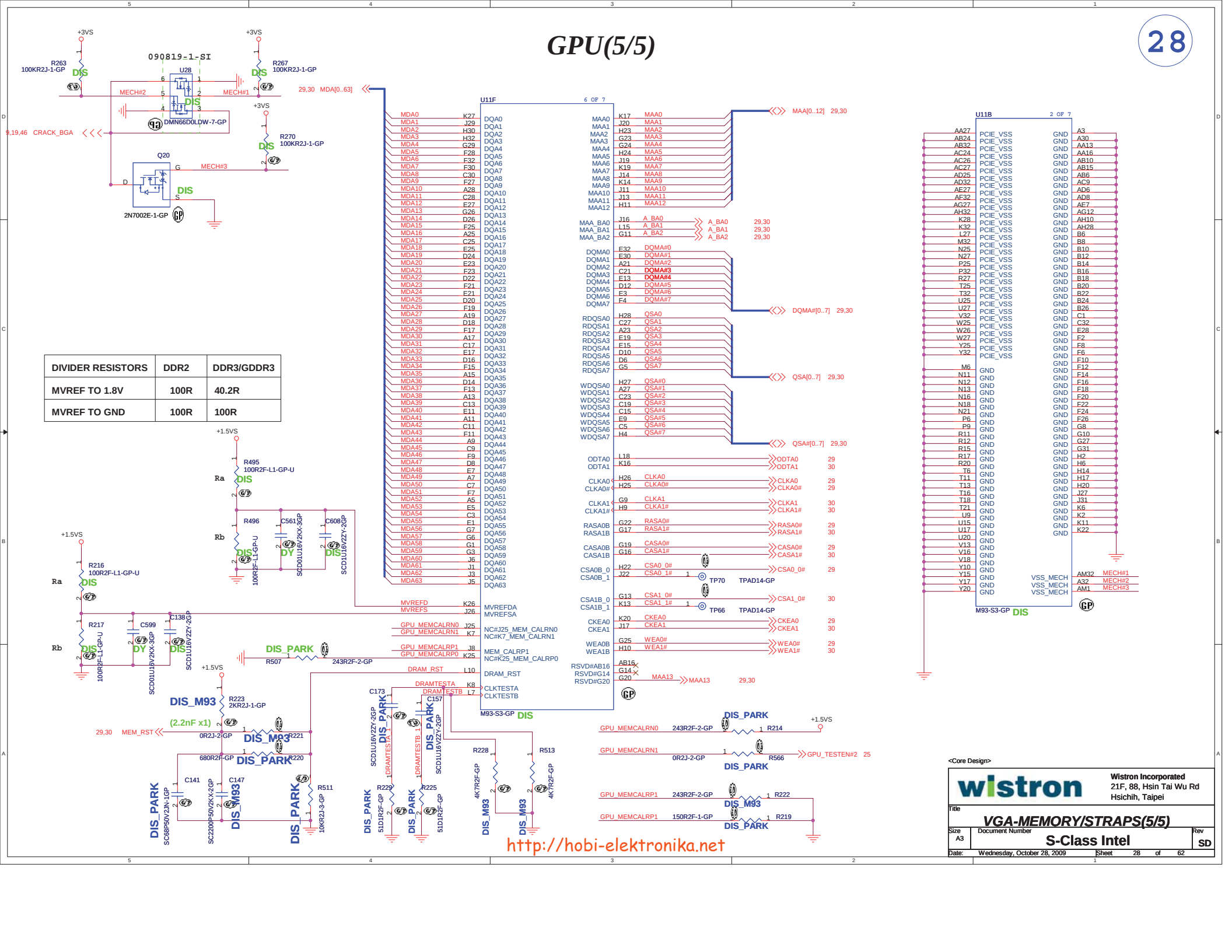
Title: VGA-POWER/GND(4/5)

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 27 of 62

GPU(5/5)

DIVIDER RESISTORS	DDR2	DDR3/GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



<Core Design>

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Title: VGA-MEMORY/STRAPS(5/5)

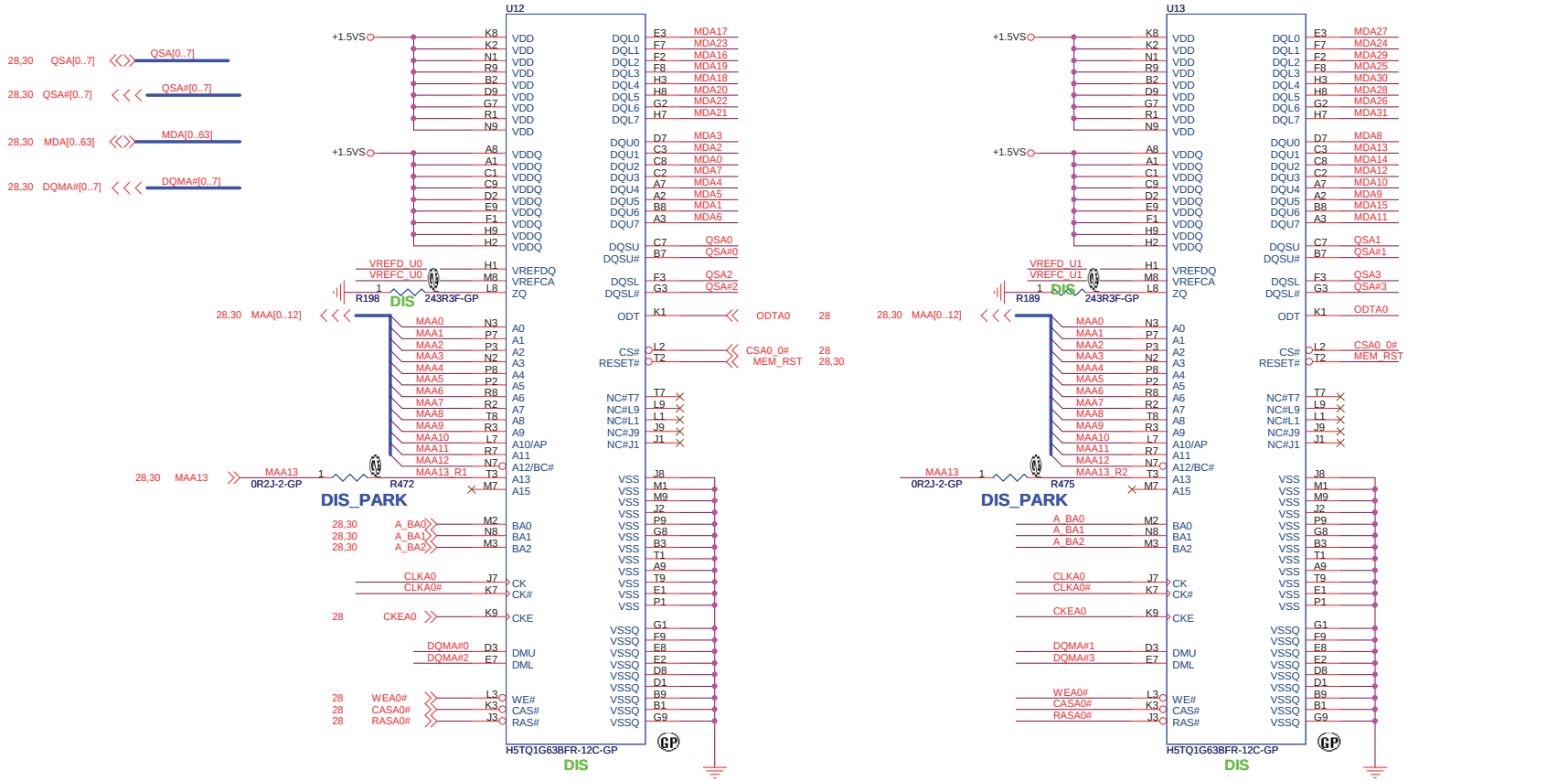
Size: A3 | Document Number: S-Class Intel | Rev: SD

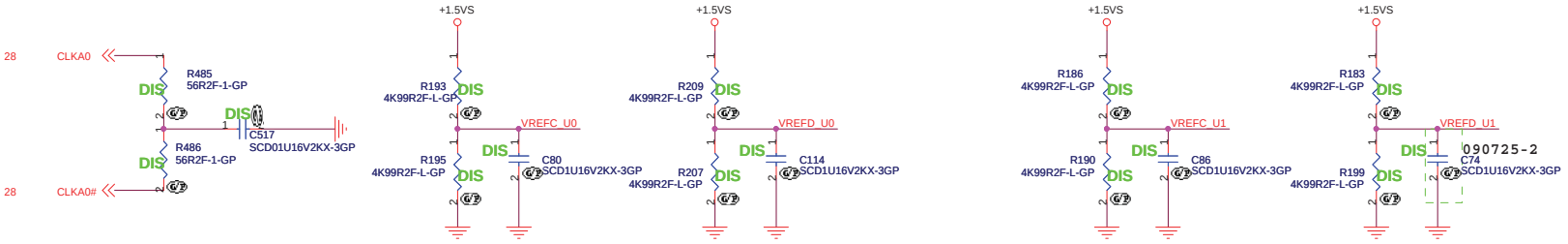
Date: Wednesday, October 28, 2009 | Sheet 28 of 62

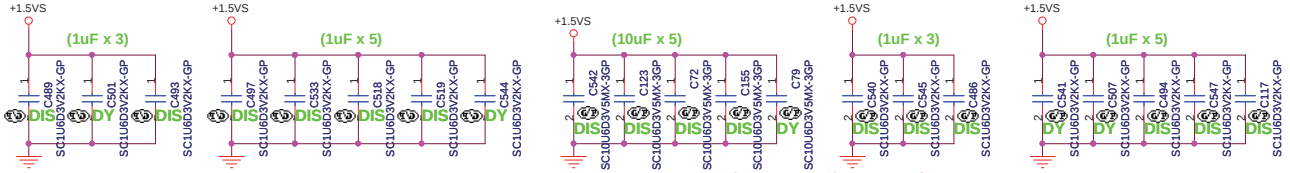
VRAM DDR3 (1/2)

256MB/512MB DDR3

29







http://hobi-elektronika.net

<Core Design>

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Title: VGA-MEMORY/STRAPS(2/4)

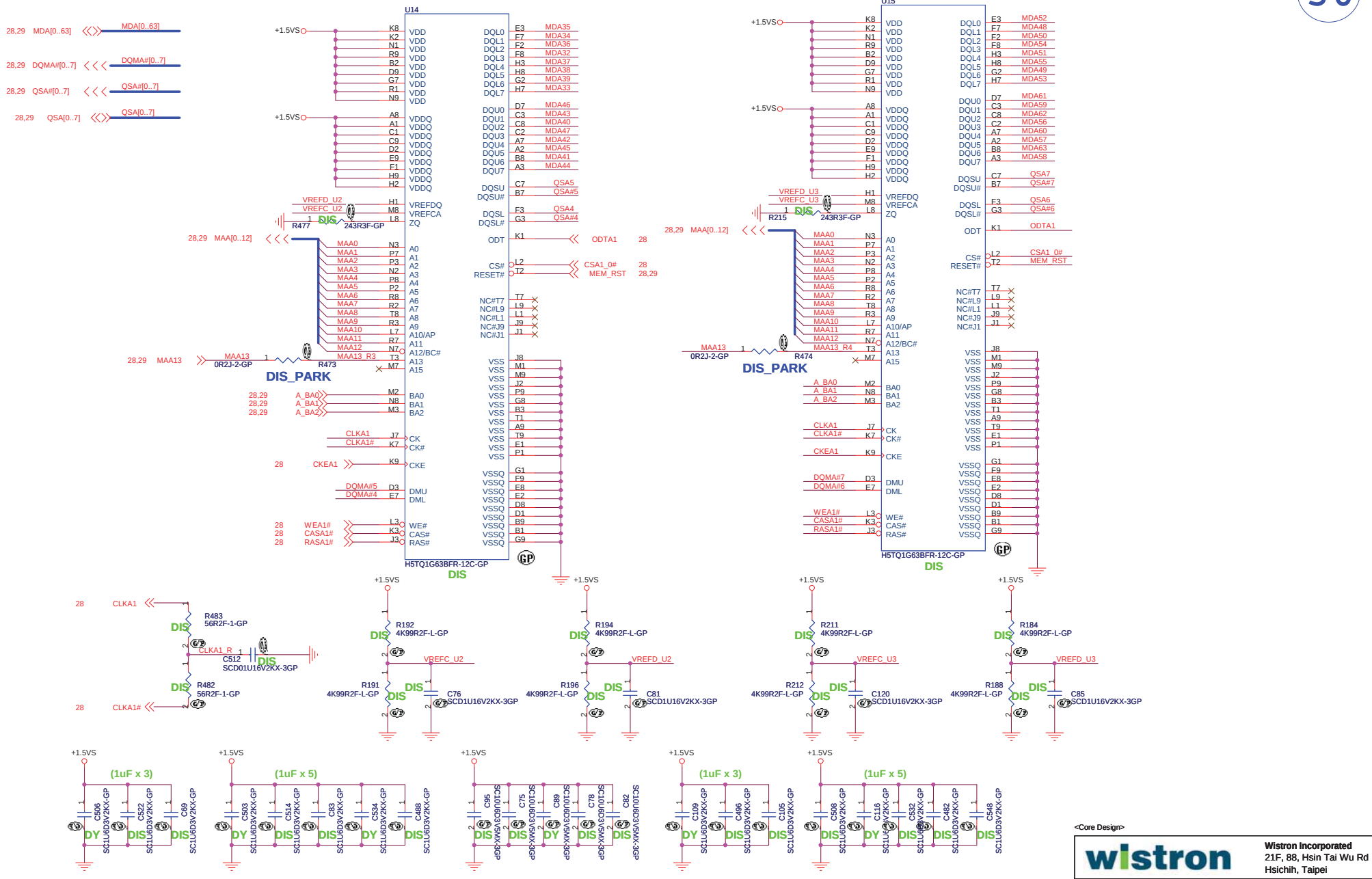
Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 29 of 62

VRAM DDR3 (2/2)

256MB/512MB DDR3

30



<Core Design>

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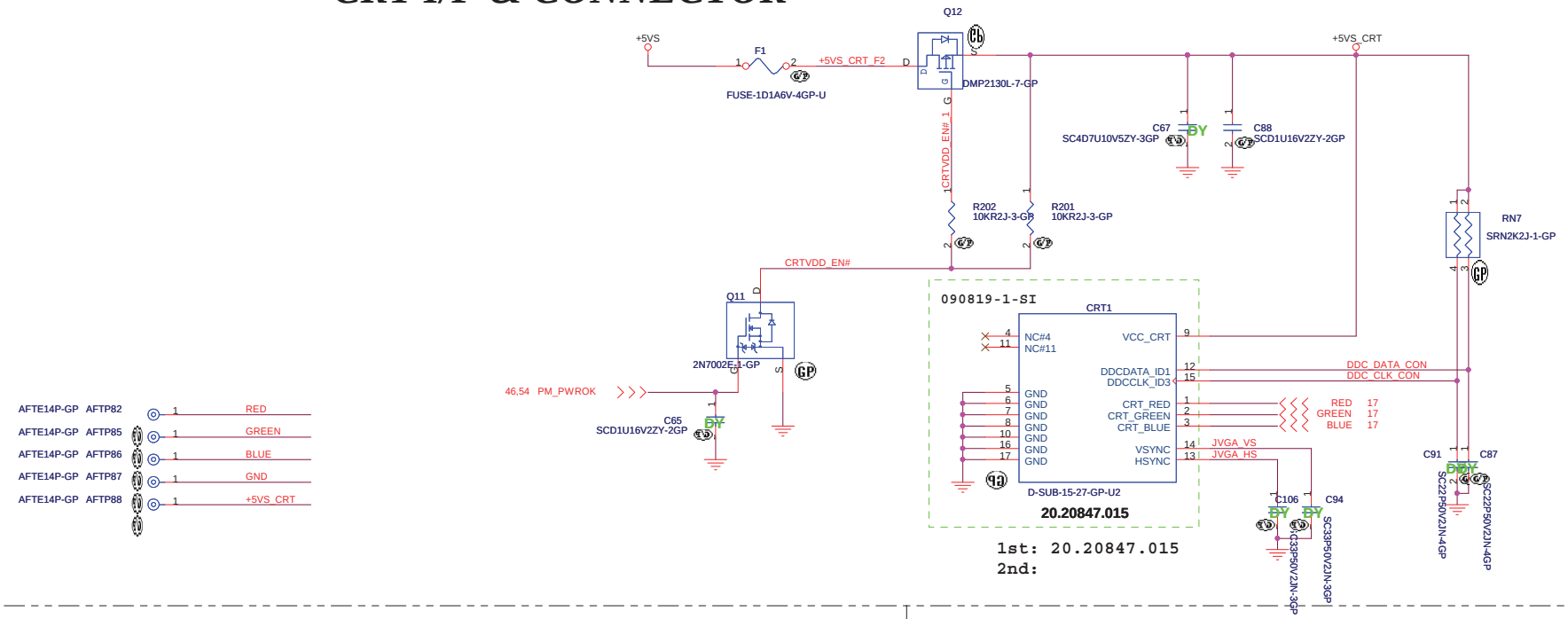
Hsichih, Taipei

Title: VGA-MEMORY/STRAPS(4/4)

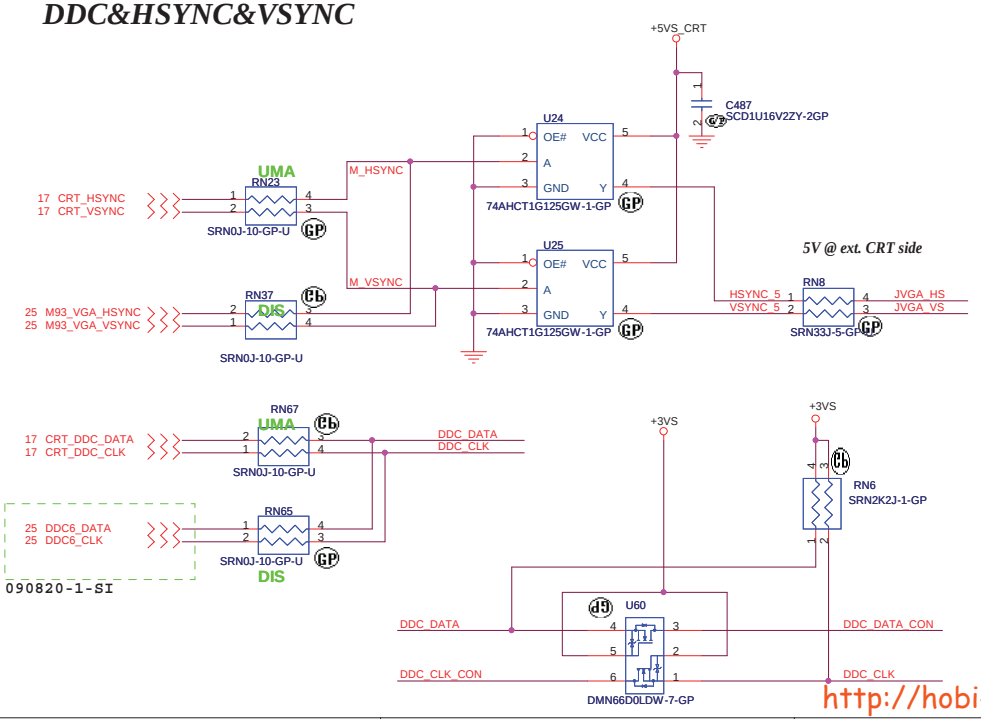
Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 30 of 62

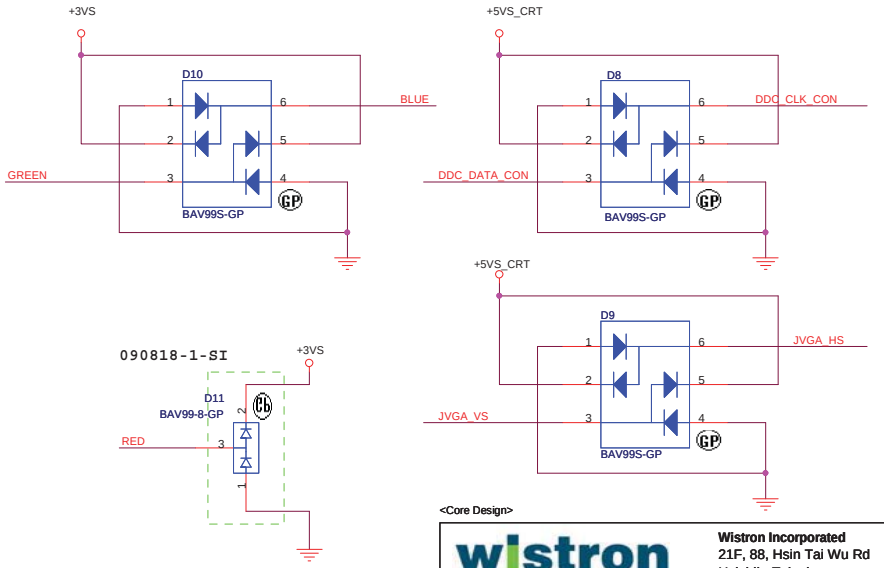
CRT I/F & CONNECTOR



DDC&HSYNC&VSYNC



ESD



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CRT Connector

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 31 of 62

LVDS CONNECTOR

LCD / INVERTER INTERFACE / CAMERA

20.F1619.040

1st: 20.F1619.040

2nd:

	SIZE_DET0 (Pin17)
17.3"	0
15.6"	1

Camera Power&Interface

Layout 40 mil

LCD Power&Discharge

<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

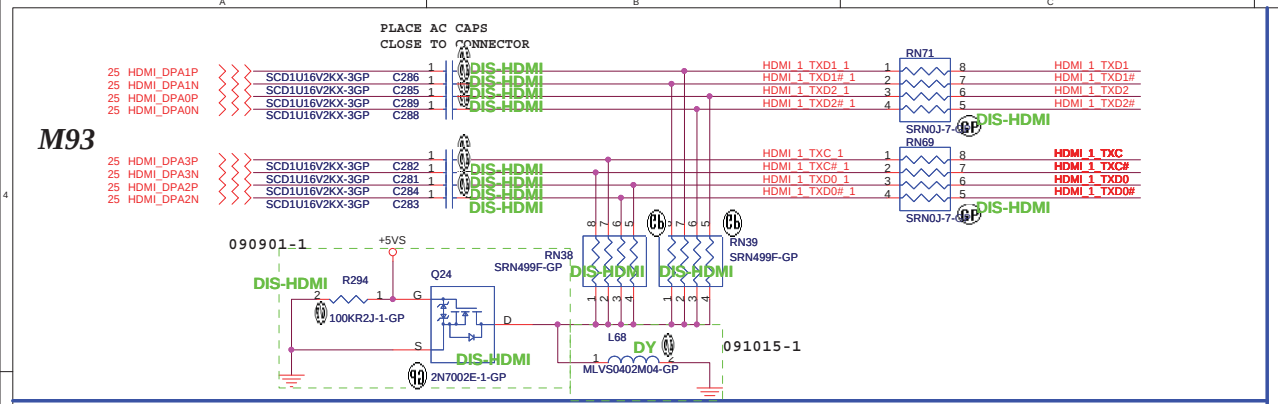
Title: LCD/Inverter Connector/CAM/LED

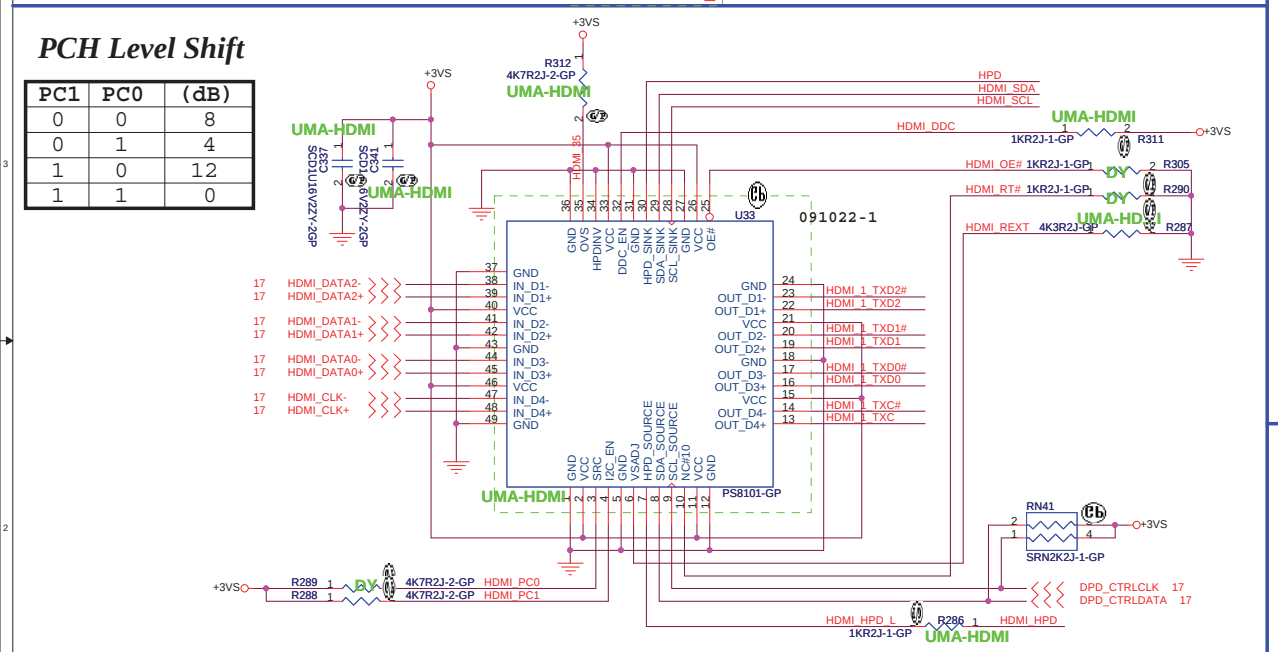
Size: Custom | Document Number: S-Class Intel | Rev: SD

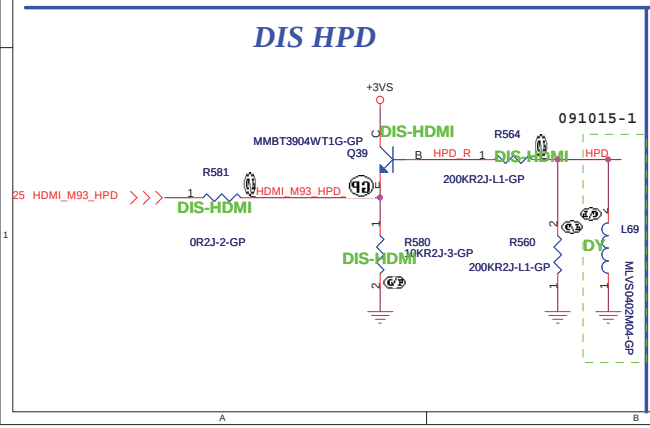
Date: Wednesday, October 28, 2009 | Sheet 32 of 62

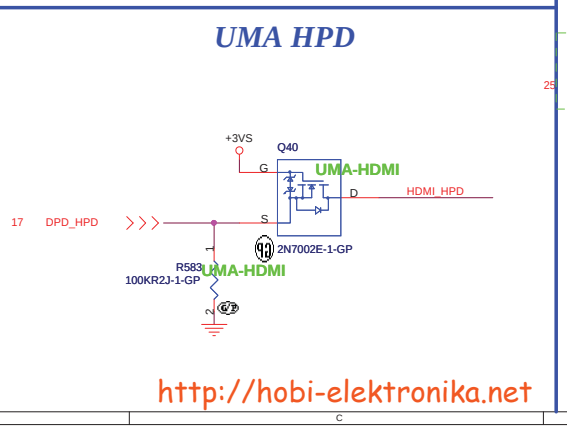
HDMI CONNECTOR

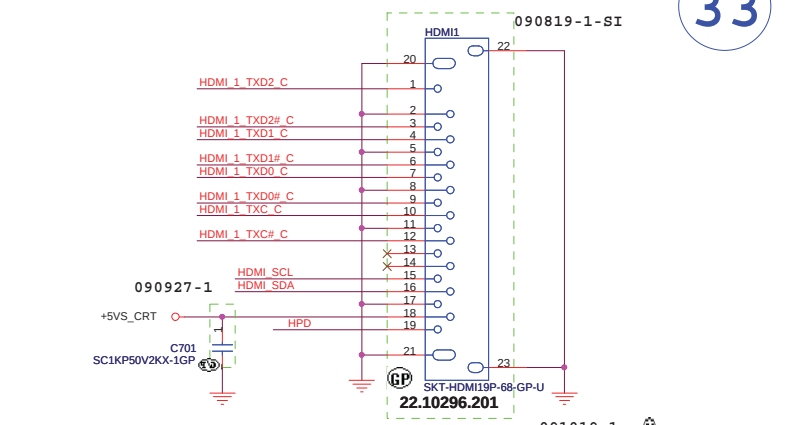
33

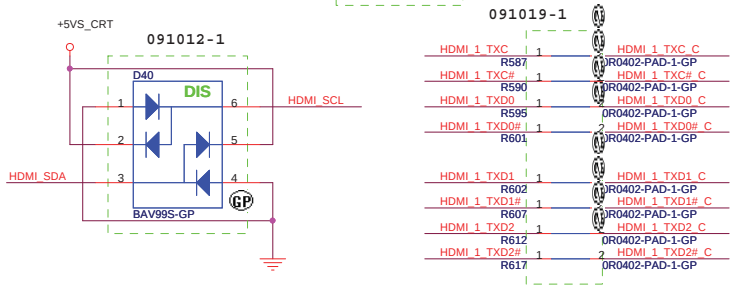


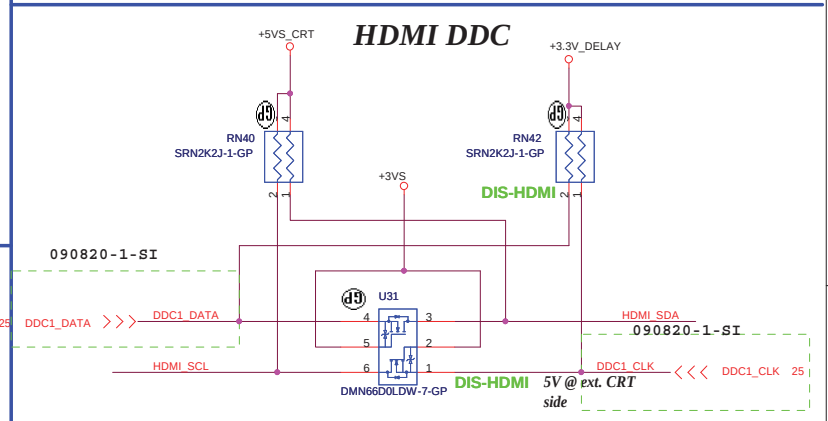












<Core Design>

wistron

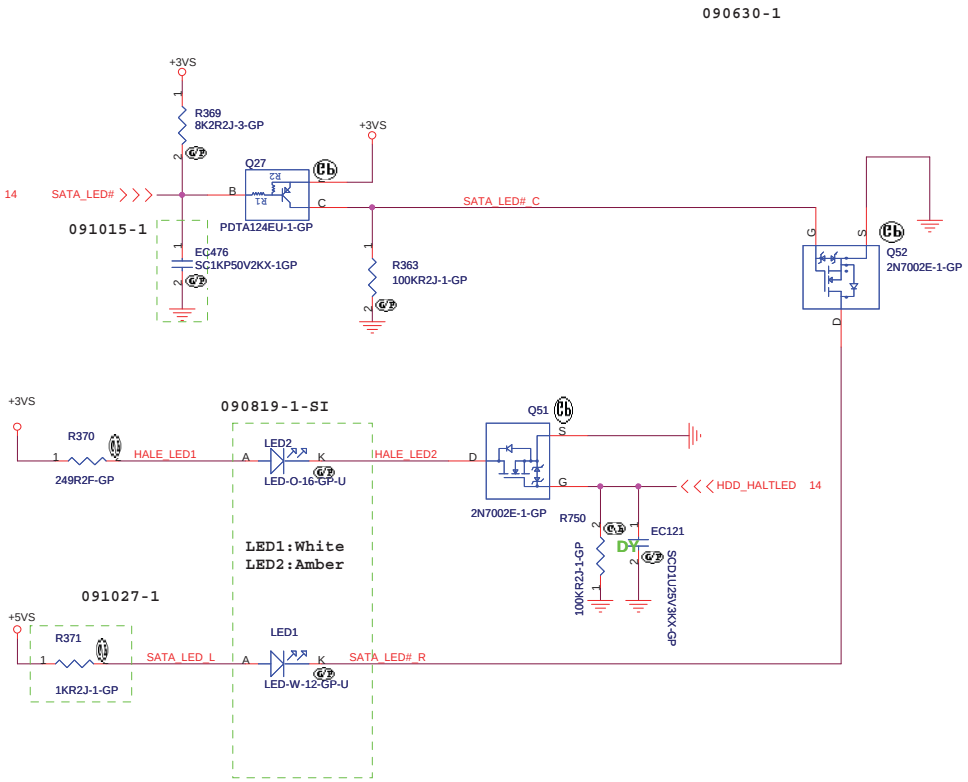
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HDMI CONN.

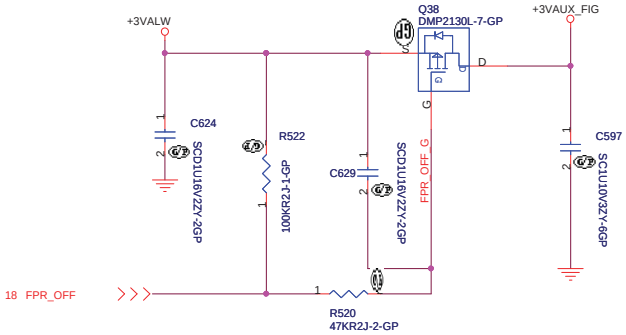
Size: A3 | Document Number: S-Class Intel | Rev: SD

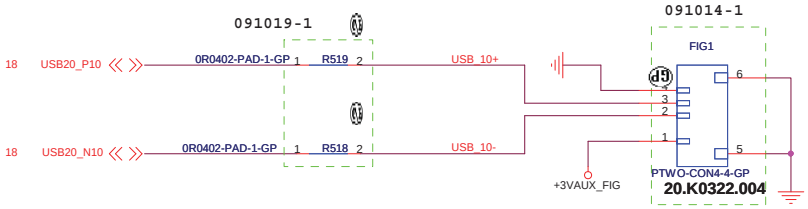
Date: Wednesday, October 28, 2009 | Sheet 33 of 62

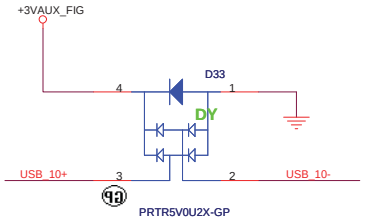
SATA LED FOR HDD

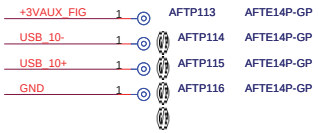


Fingerprint









<Core Design>

wistron

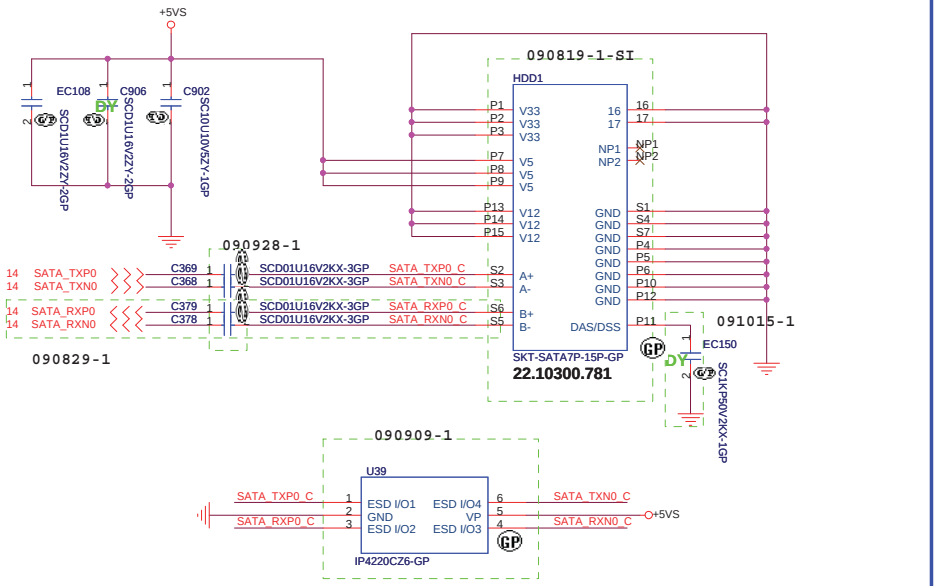
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SATA&CAP LED&GOLDEN FINGER

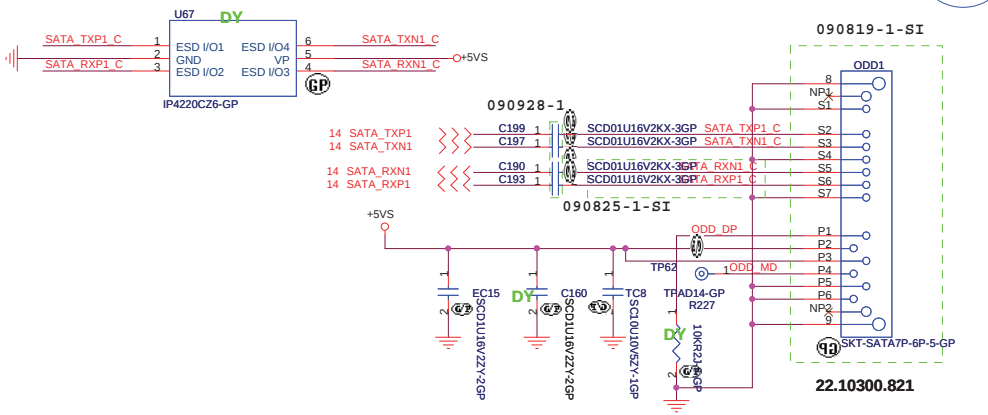
Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 34 of 62

SATA HD Connector

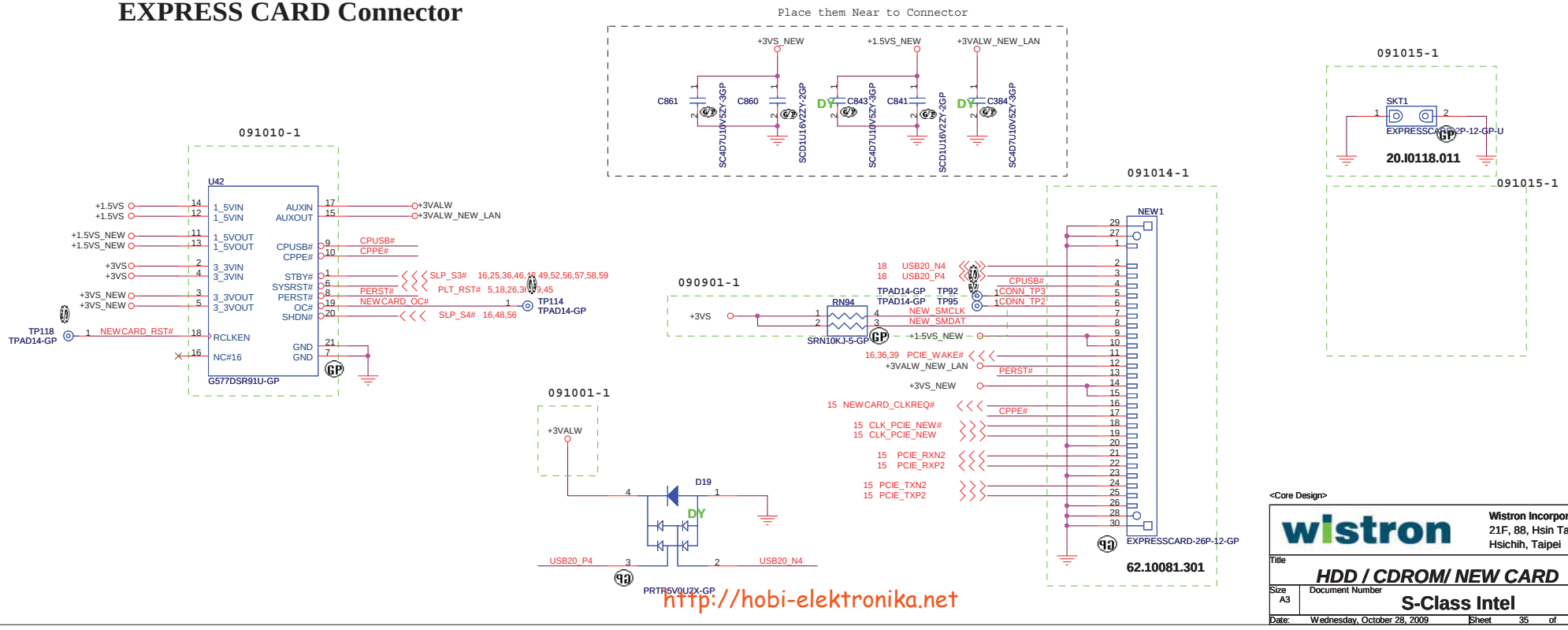


ODD Connector



35

EXPRESS CARD Connector



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HDD / CDROM/ NEW CARD

Size	Document Number	Rev
A3	S-Class Intel	SD

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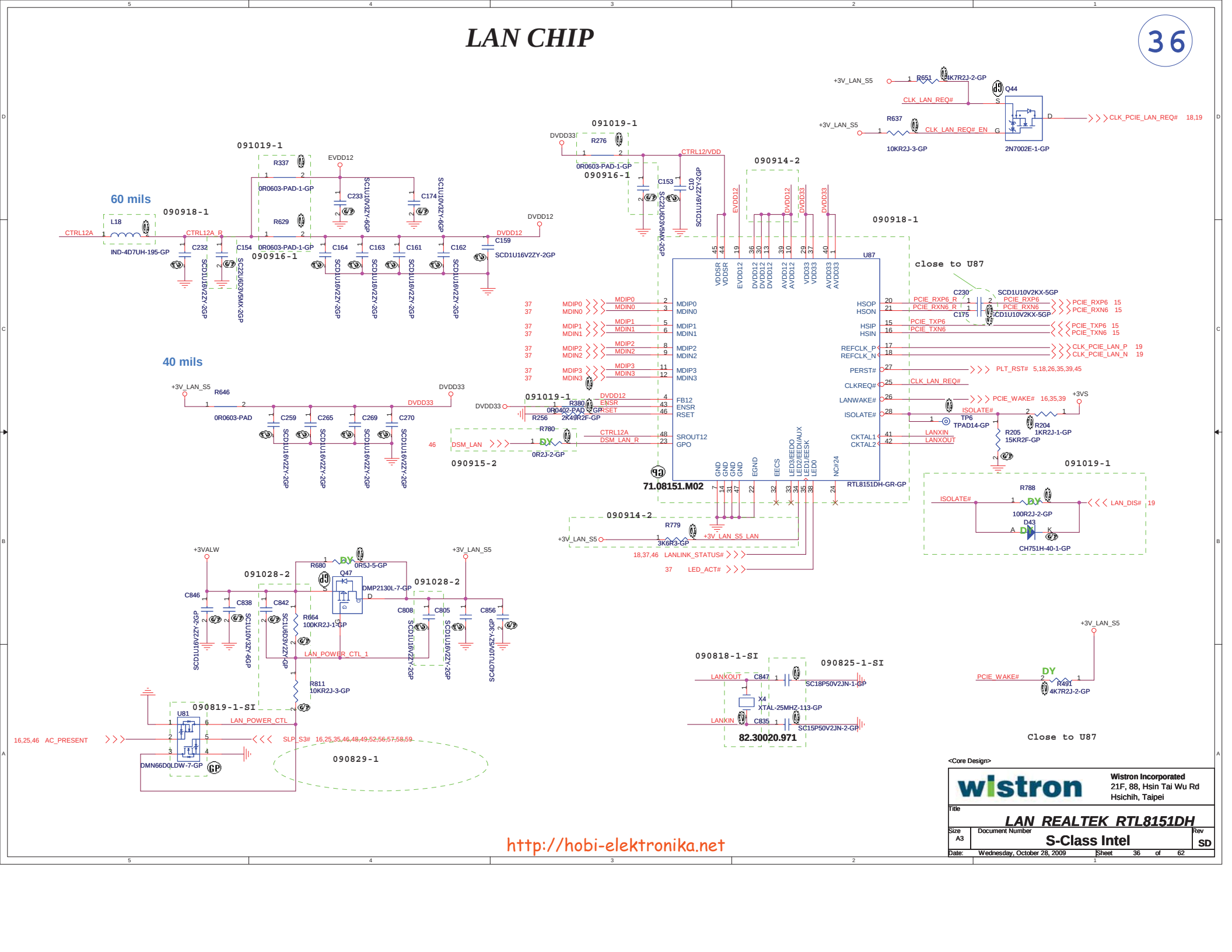
LAN CHIP



<Core Design>

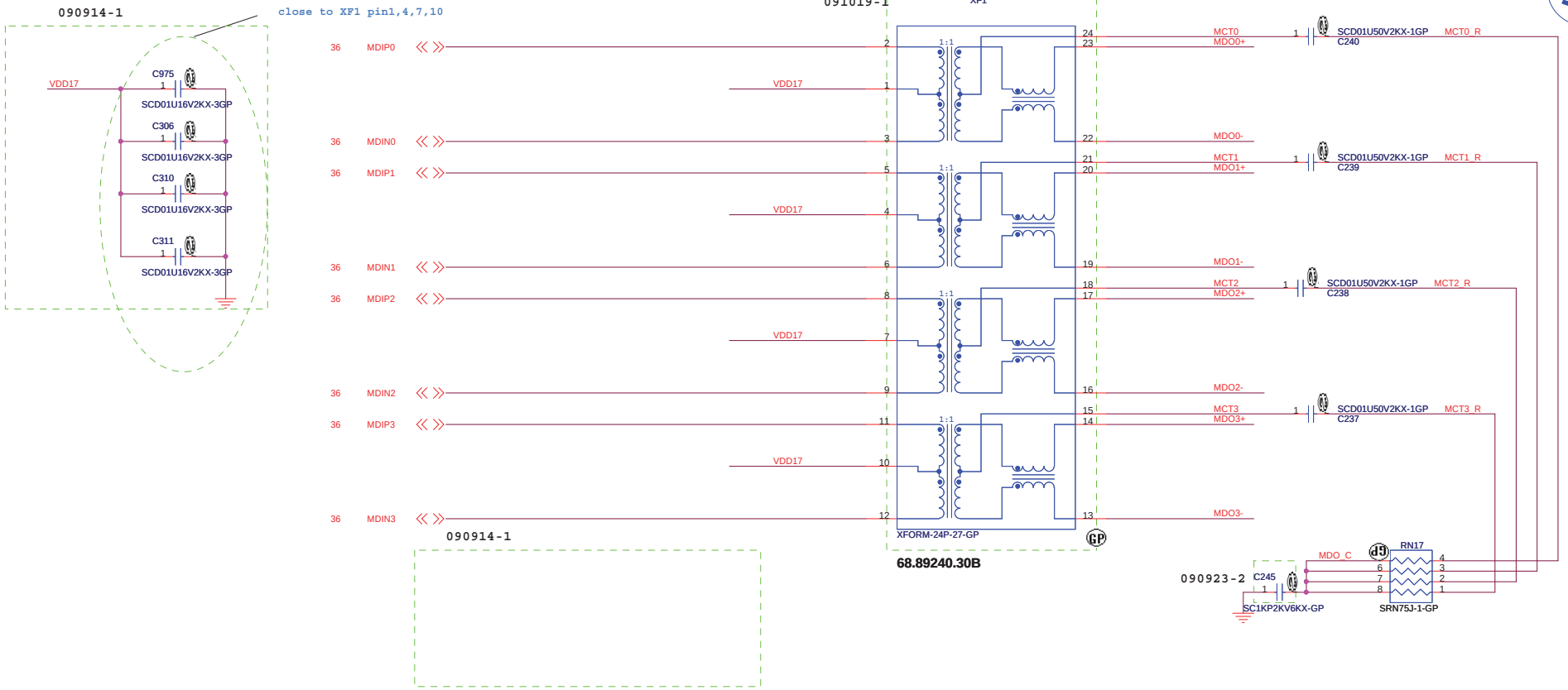
wistron

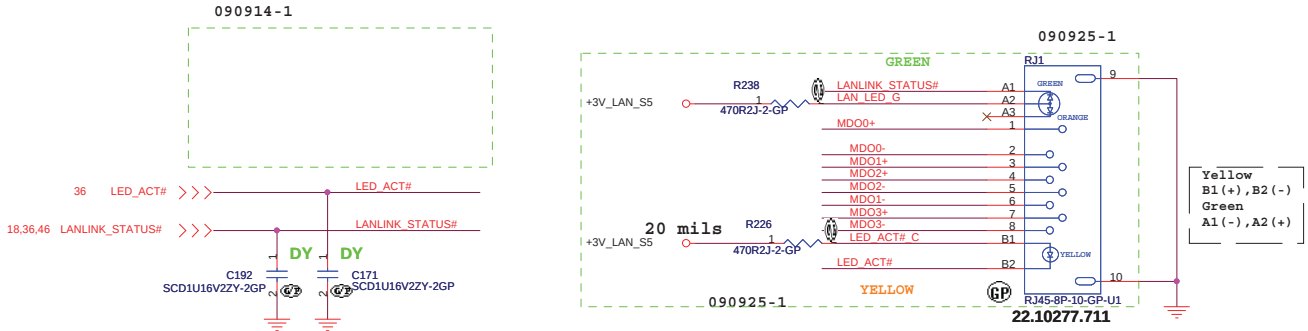
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LAN_REALTEK_RTL8151DH

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 36 of 62





IF NOT OVER CLOCKING, LED_ACT# WILL ACT HIGH Check LAN chip for LED_ACT# function on RJ45 connector pin define.

<Core Design>

wistron

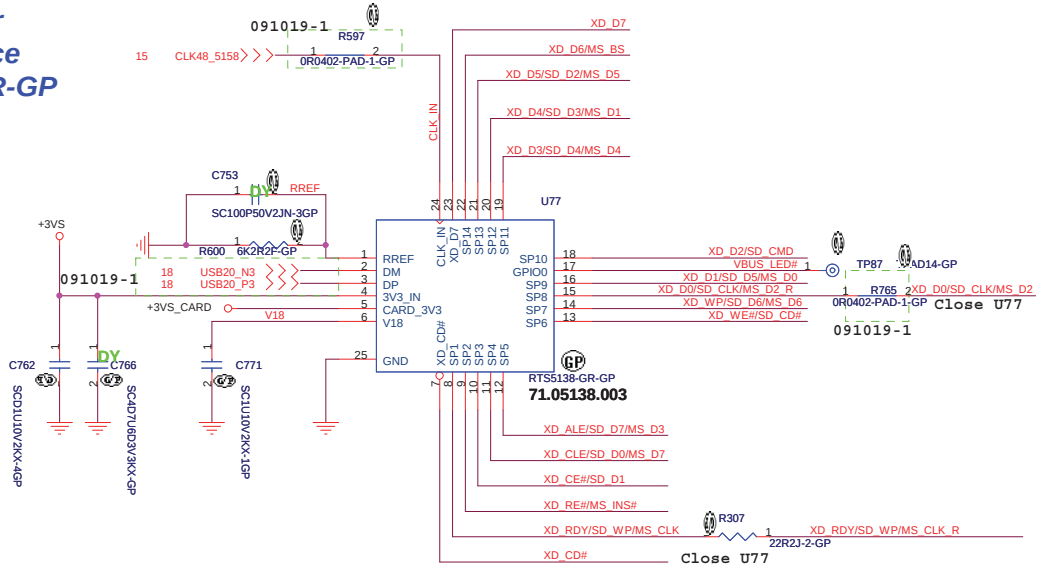
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Magnetic & RJ45

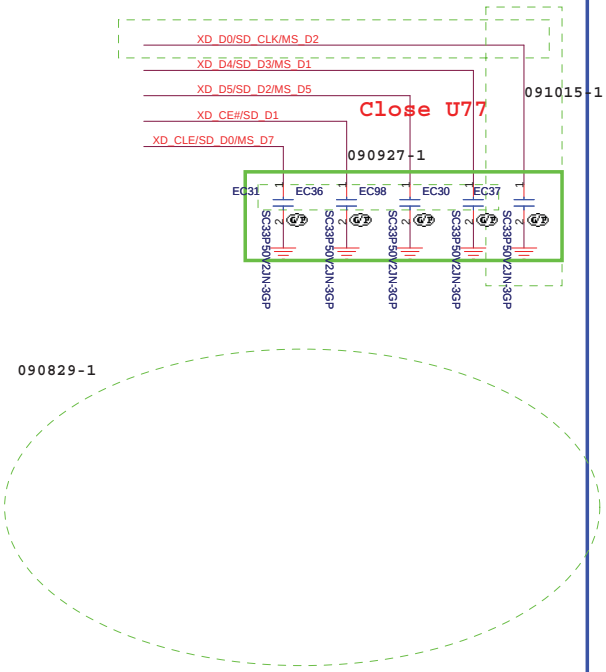
Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 37 of 62

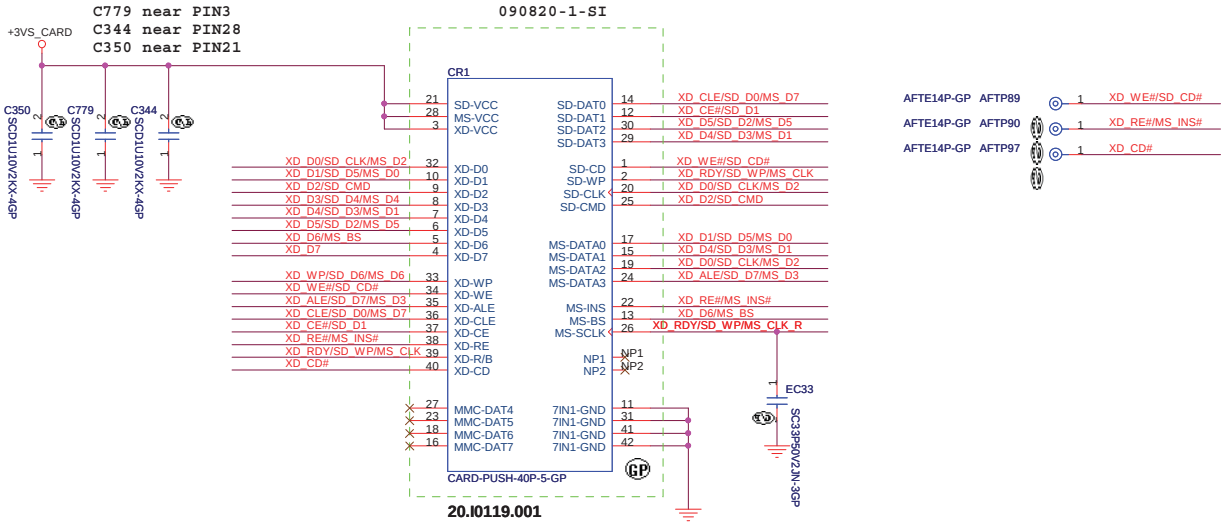
Card Reader
USB Interface
RTS5138-GR-GP



EMI Reserve Cap



4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

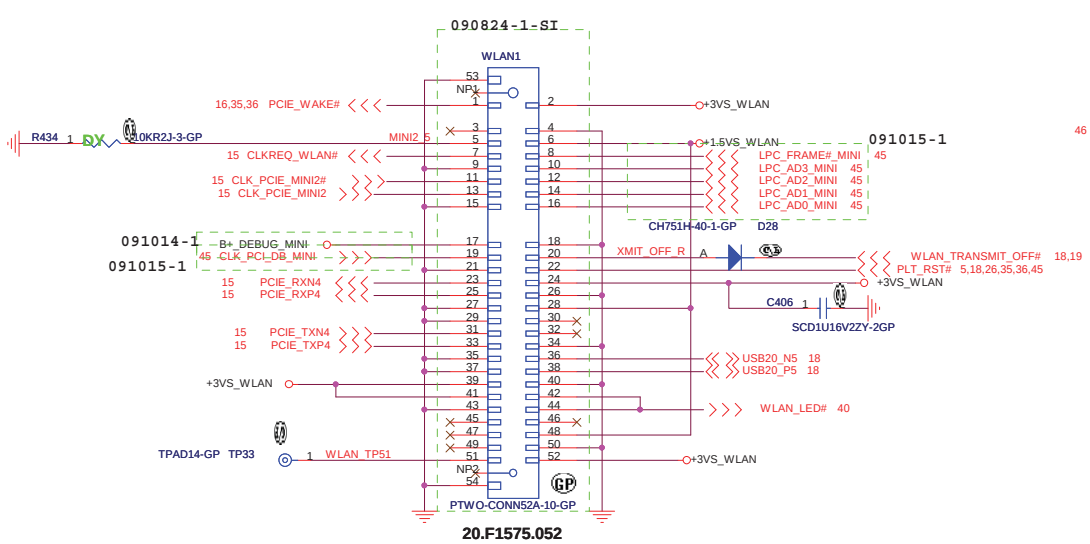
Title: CardReader RTS5138

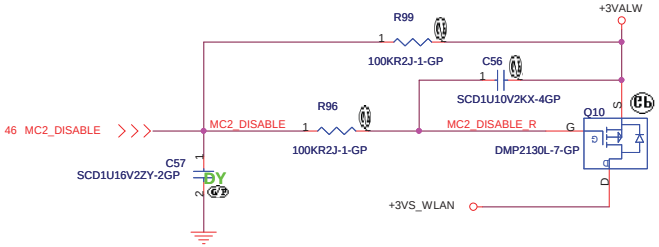
Size	Document Number	Rev
A3	S-Class Intel	SD

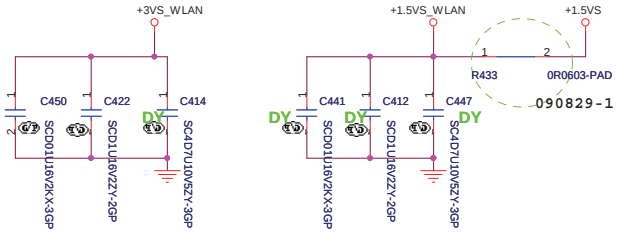
Date: Wednesday, October 28, 2009 Sheet 38 of 62

Mini-Card--WLAN

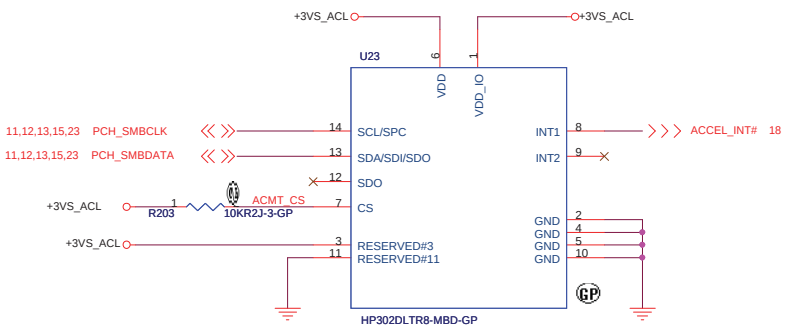
Half minicard

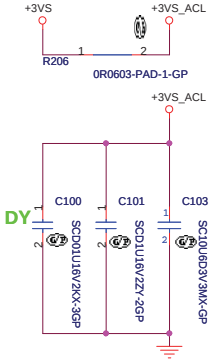






ACCELEROMETER





<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

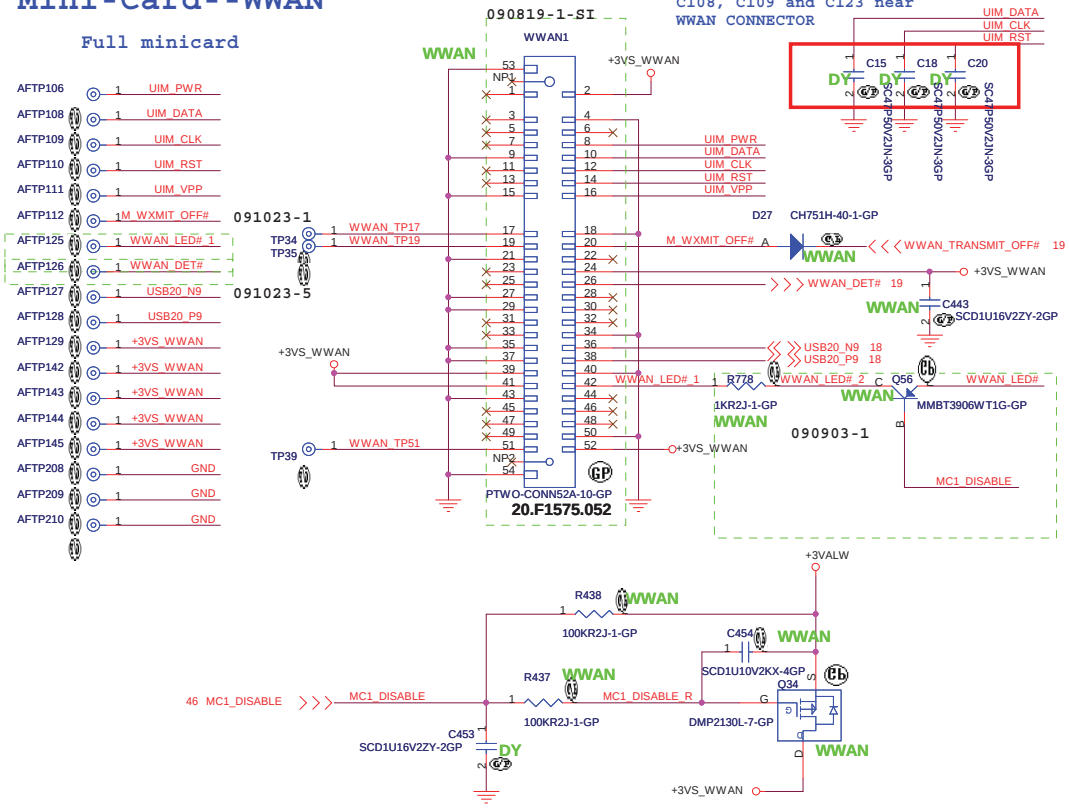
Title: Mini-Card/Accelerometer

Size: A3 | Document Number: S-Class Intel | Rev: SD

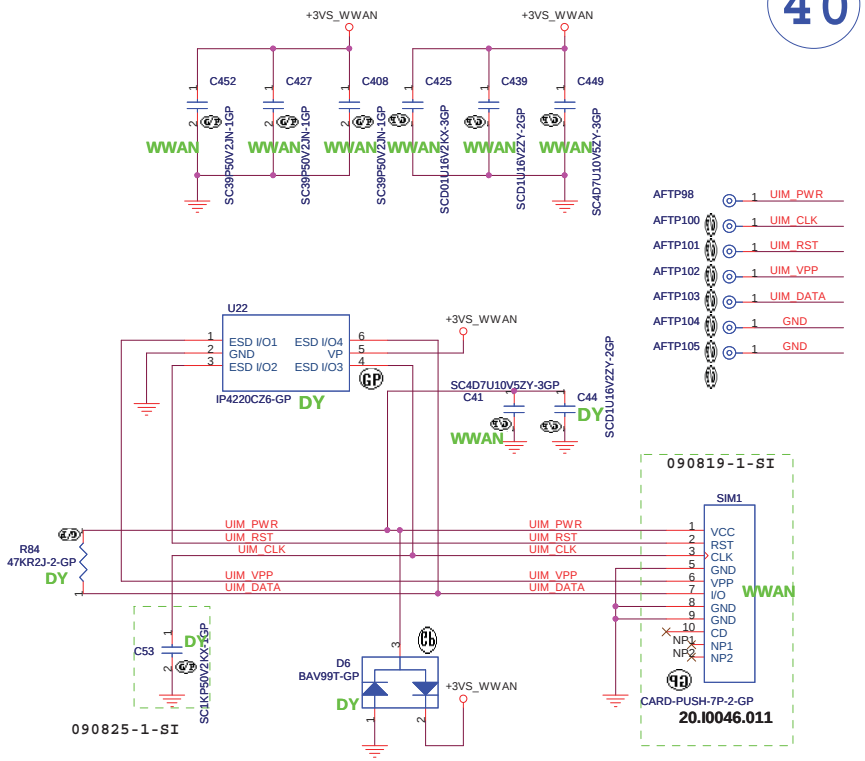
Date: Wednesday, October 28, 2009 | Sheet 39 of 62

Mini-Card--WWAN

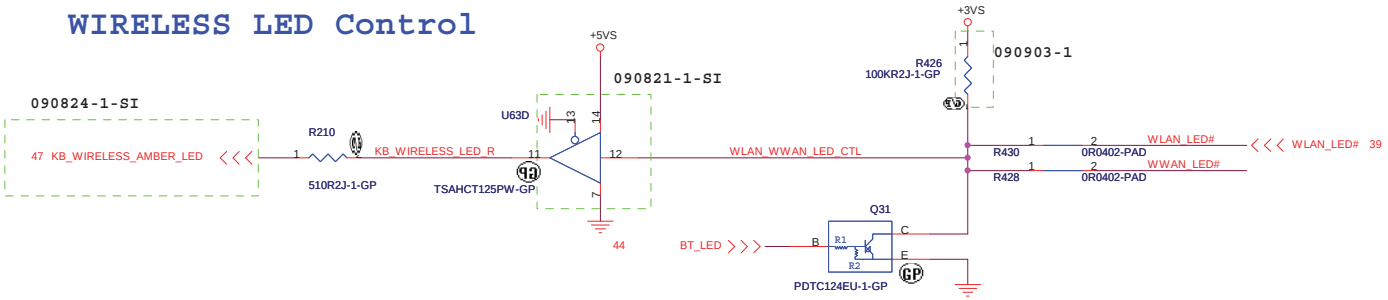
Full minicard

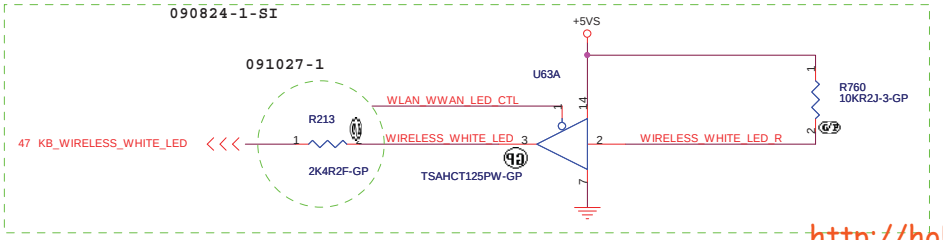


SIM Card Slot



WIRELESS LED Control





<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Mini-Card/Accelerometer

Size: A3 | Document Number: S-Class Intel | Rev: SD

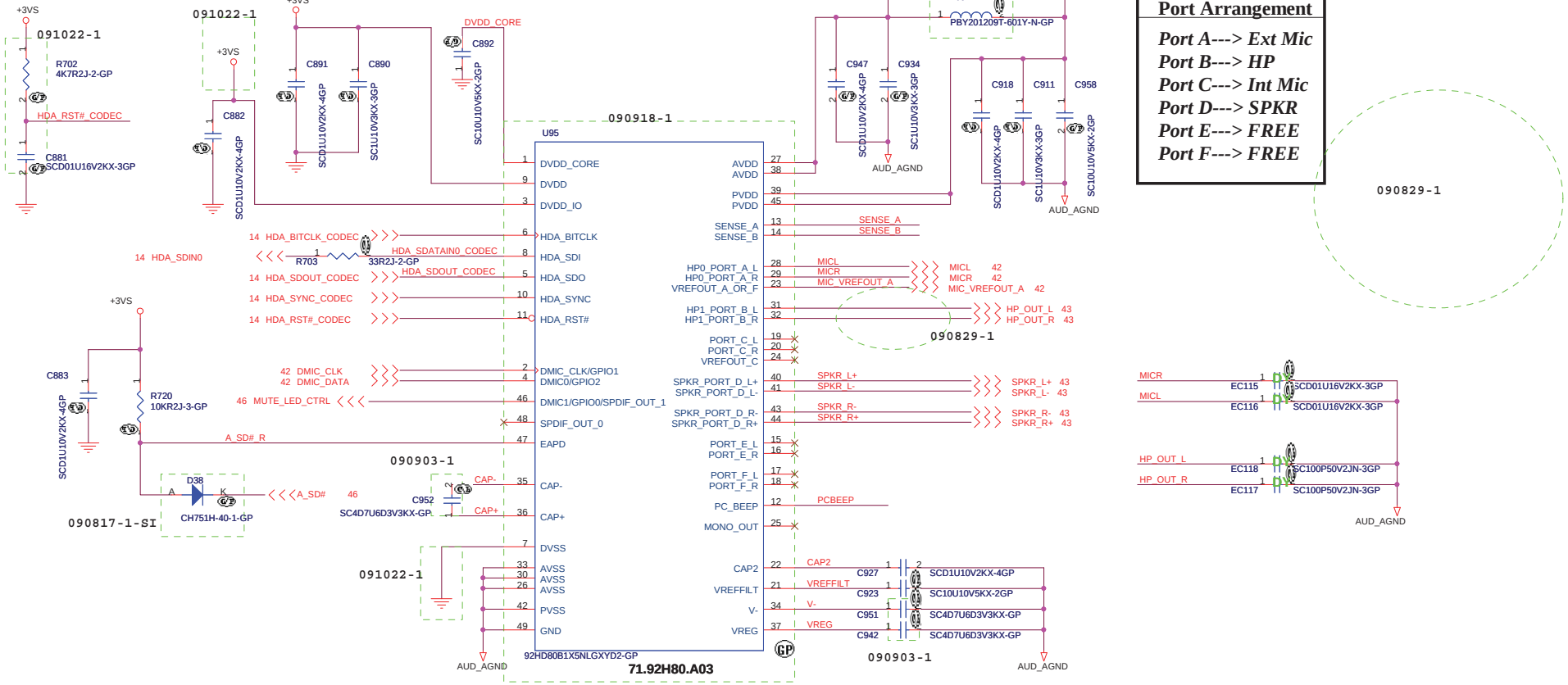
Date: Wednesday, October 28, 2009 | Sheet 40 of 62

AUDIO CODEC(92HD80)

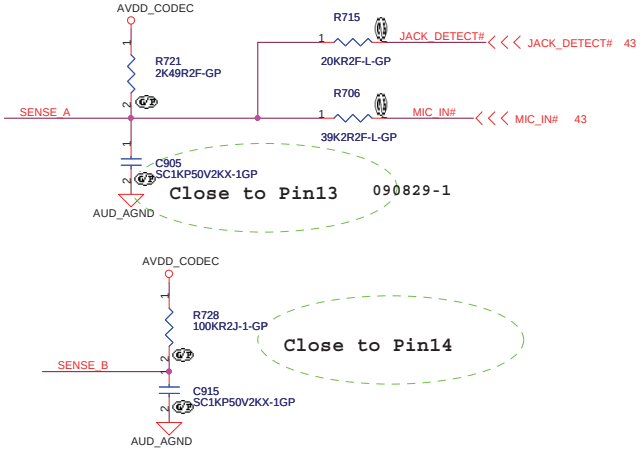
090821-1-SI

Port Arrangement

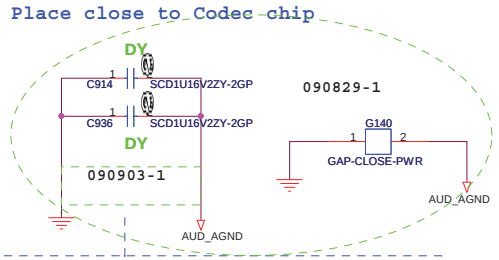
Port A---> Ext Mic
Port B---> HP
Port C---> Int Mic
Port D---> SPKR
Port E---> FREE
Port F---> FREE



SENSE Detect



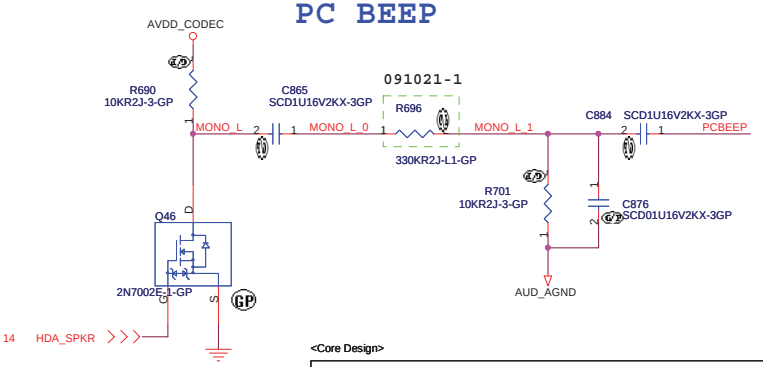
Digital GND & AUD_AGND



audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

http://hobi-elektronika.net

PC BEEP



<Core Design>

wistron

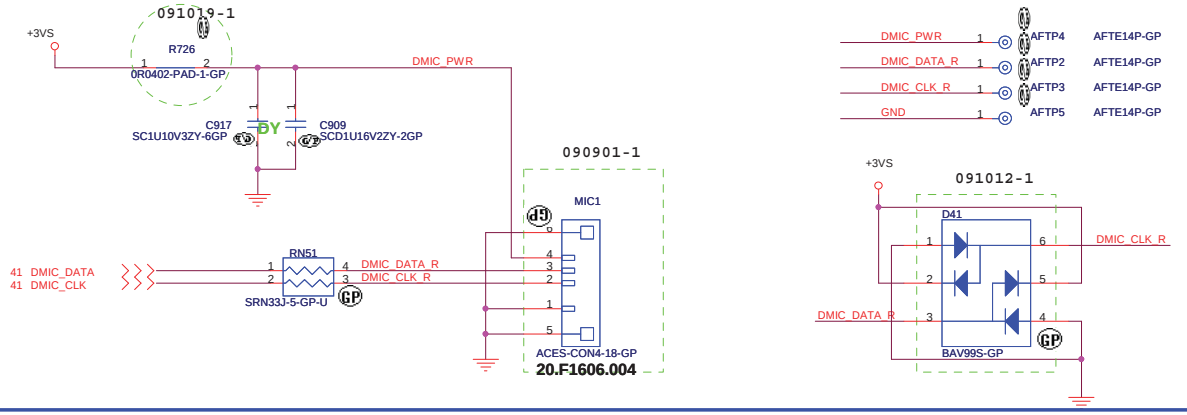
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AUDIO 92HD80 / OP AMP

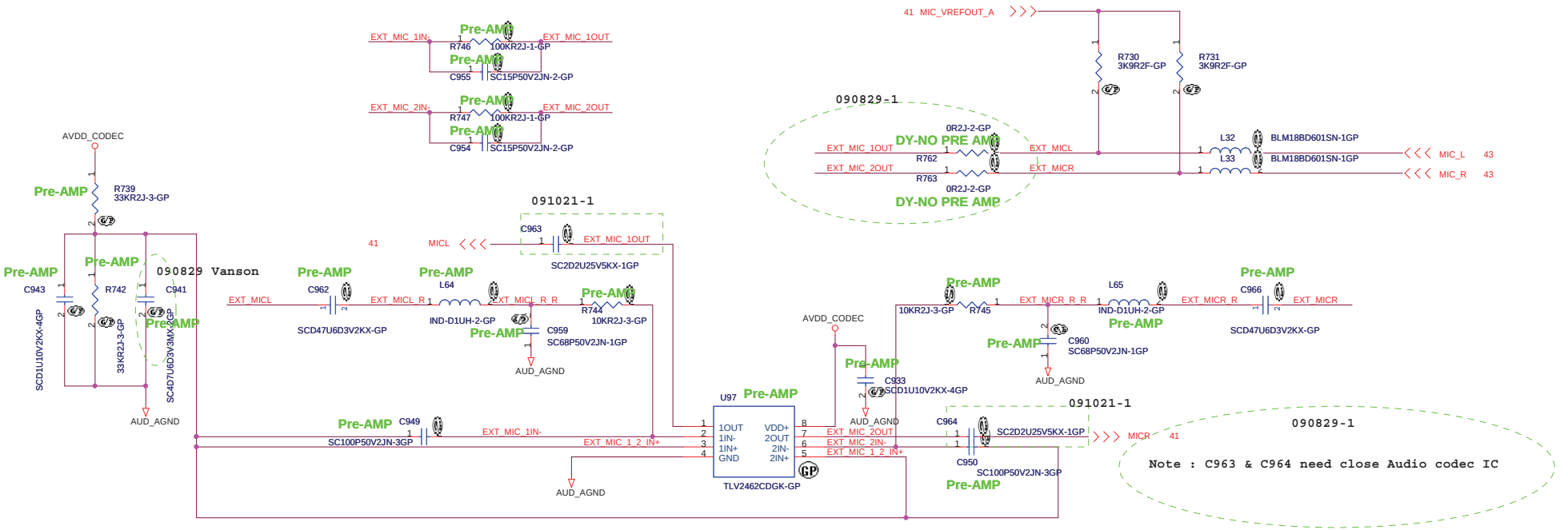
Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 41 of 62

Internal Digital MIC



Ppre-AMP. for External MIC



<Core Design>

wistron

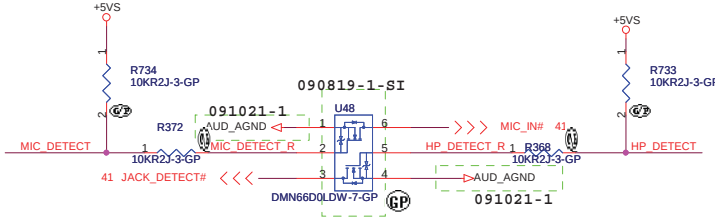
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AUDIO Pre-AMP / CONN

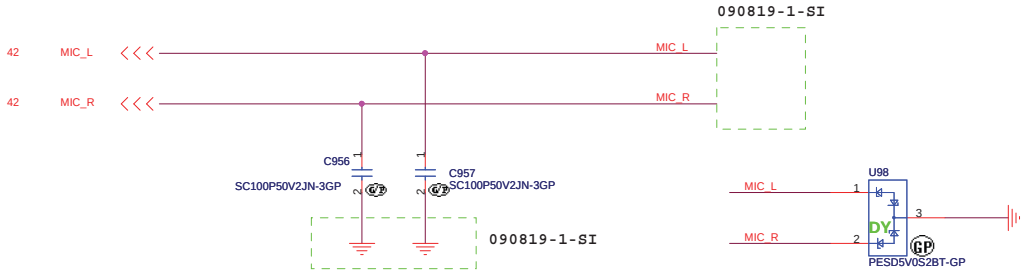
Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 42 of 62

Jack Detect

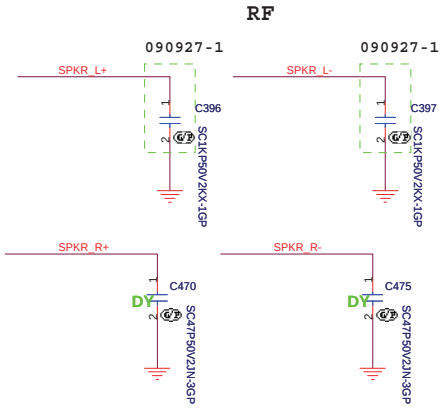


MIC IN

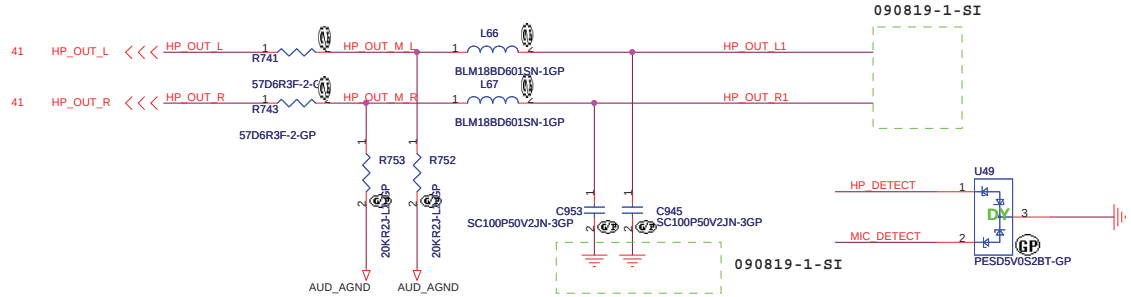


43

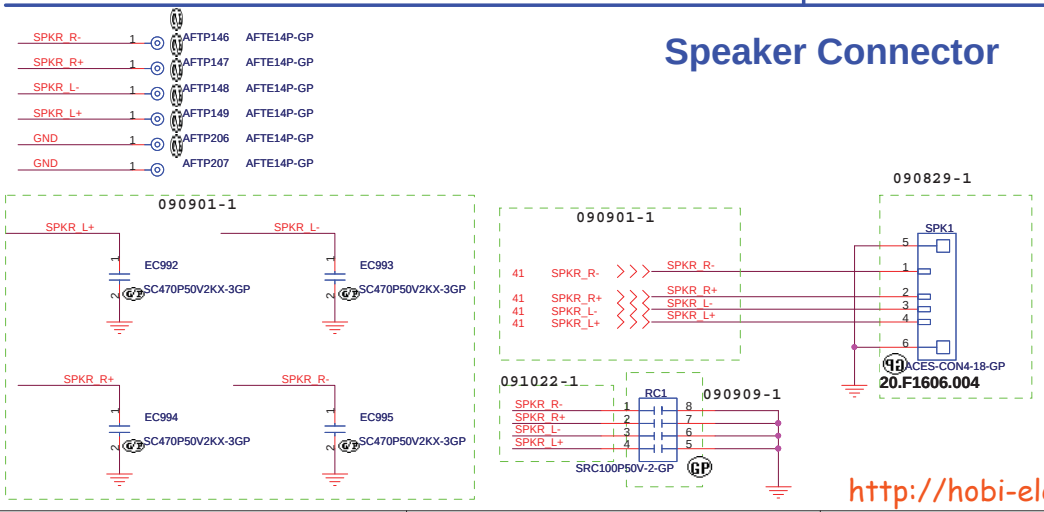
RF Reserver Cap



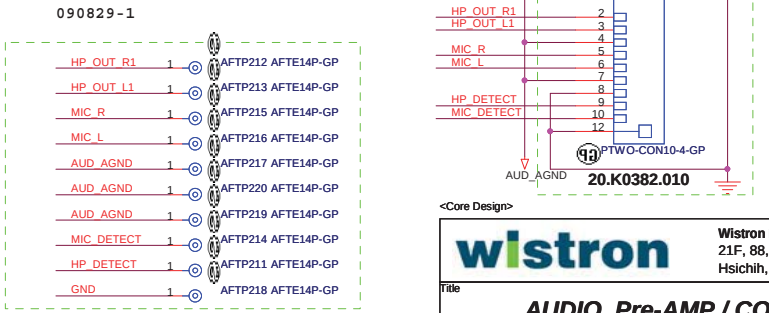
HeadPhone OUT



Speaker Connector



Audio Board Connector



<Core Design>

wistron

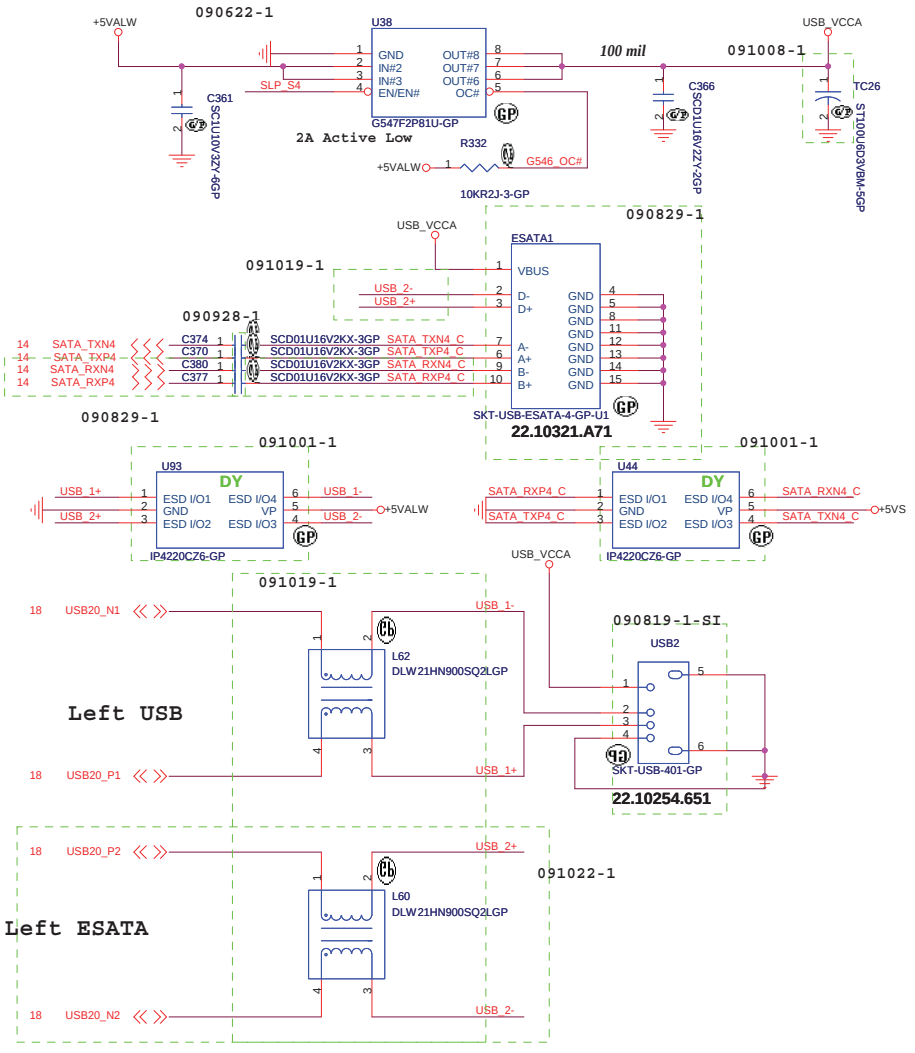
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AUDIO Pre-AMP / CONN

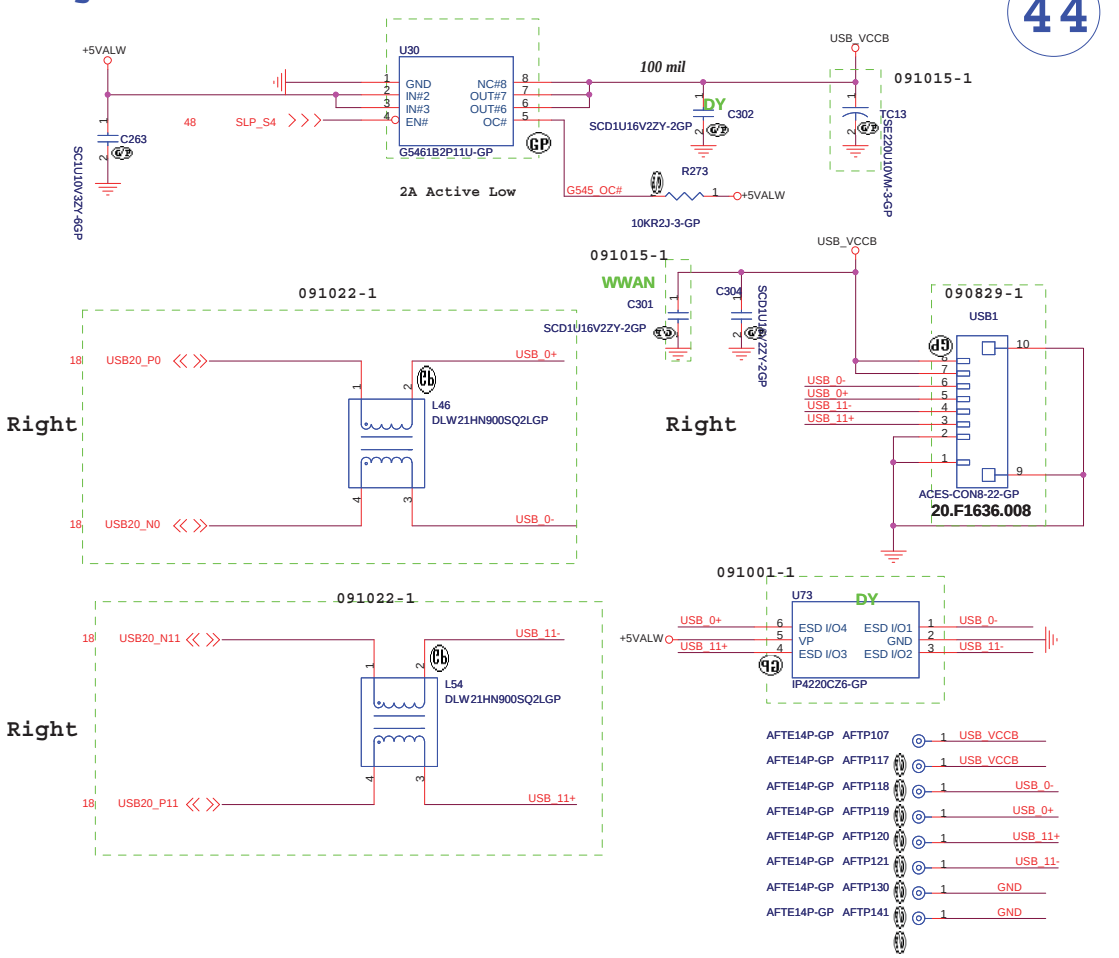
Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 43 of 62

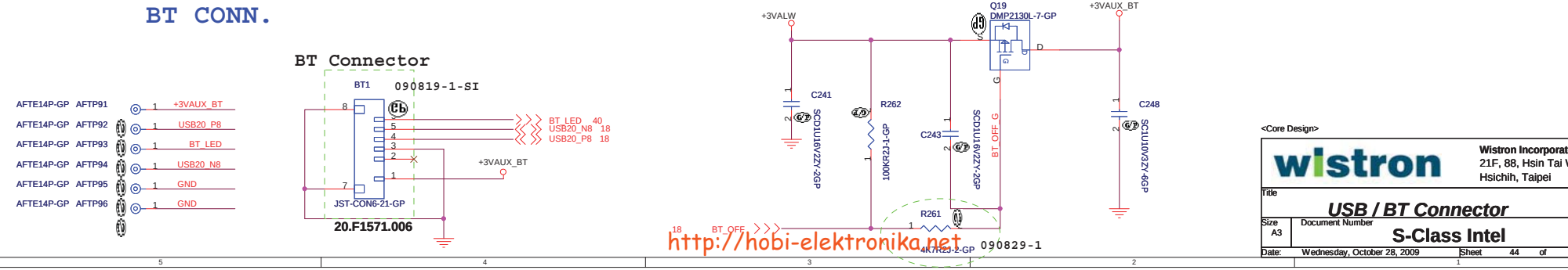
Left Side USB + ESATA Port



Right Side USB x 2



BT CONN.



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: USB / BT Connector

Size: A3 | Document Number: S-Class Intel | Rev: SD

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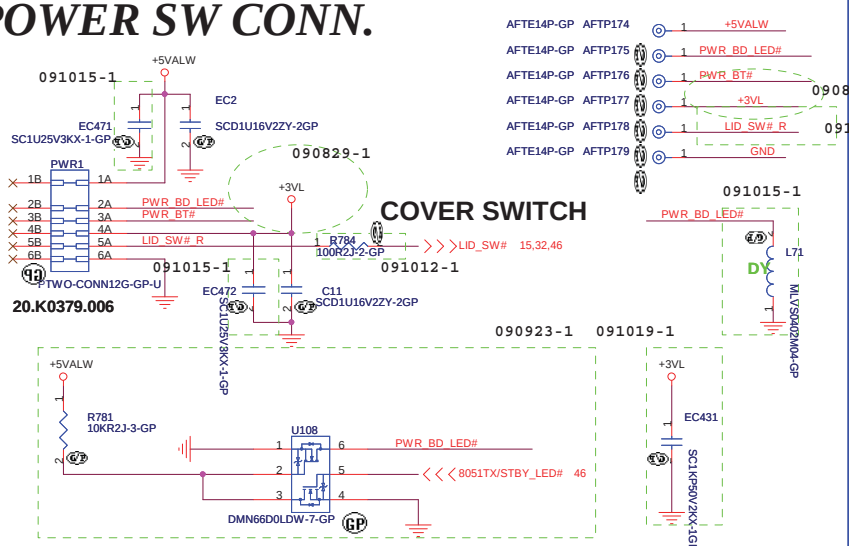
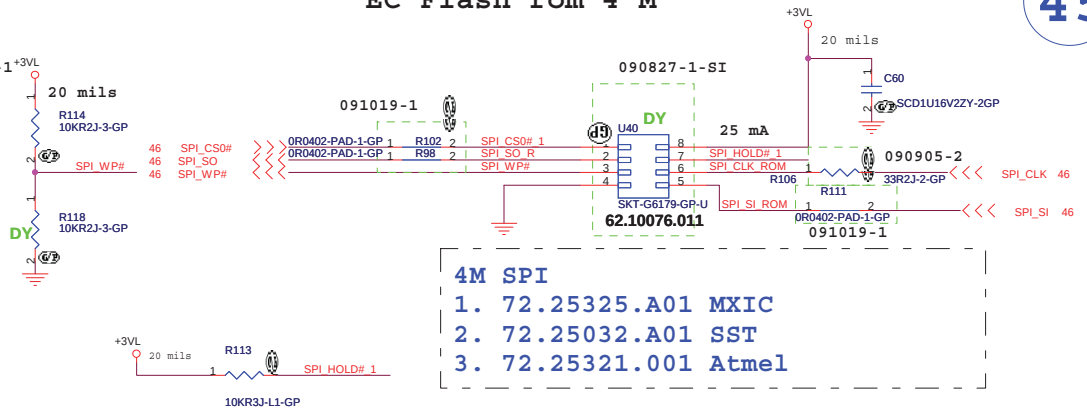
POWER SW CONN.

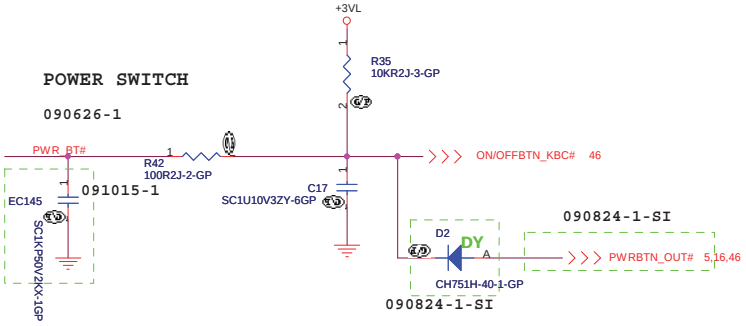


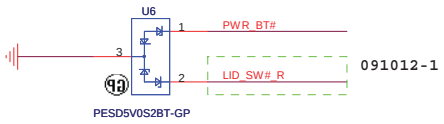
EC Flash rom 4 M



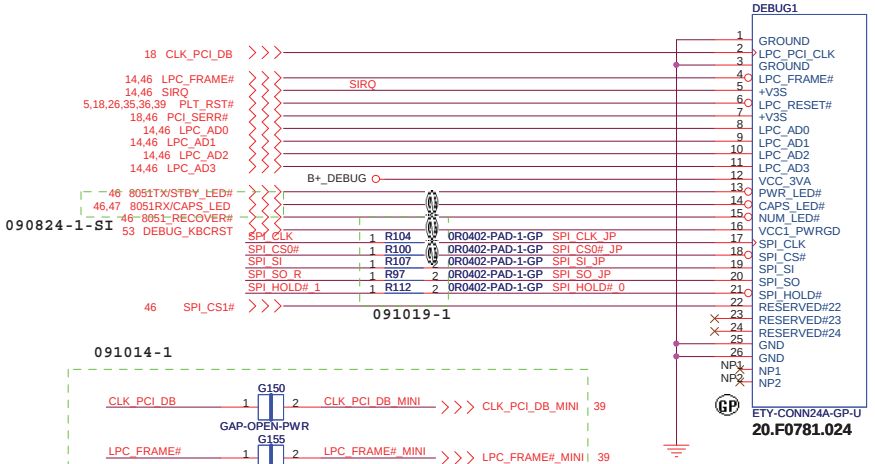
45

Power SW Circuit





24 PIN LPC DEBUG CONN.



<Core Design>

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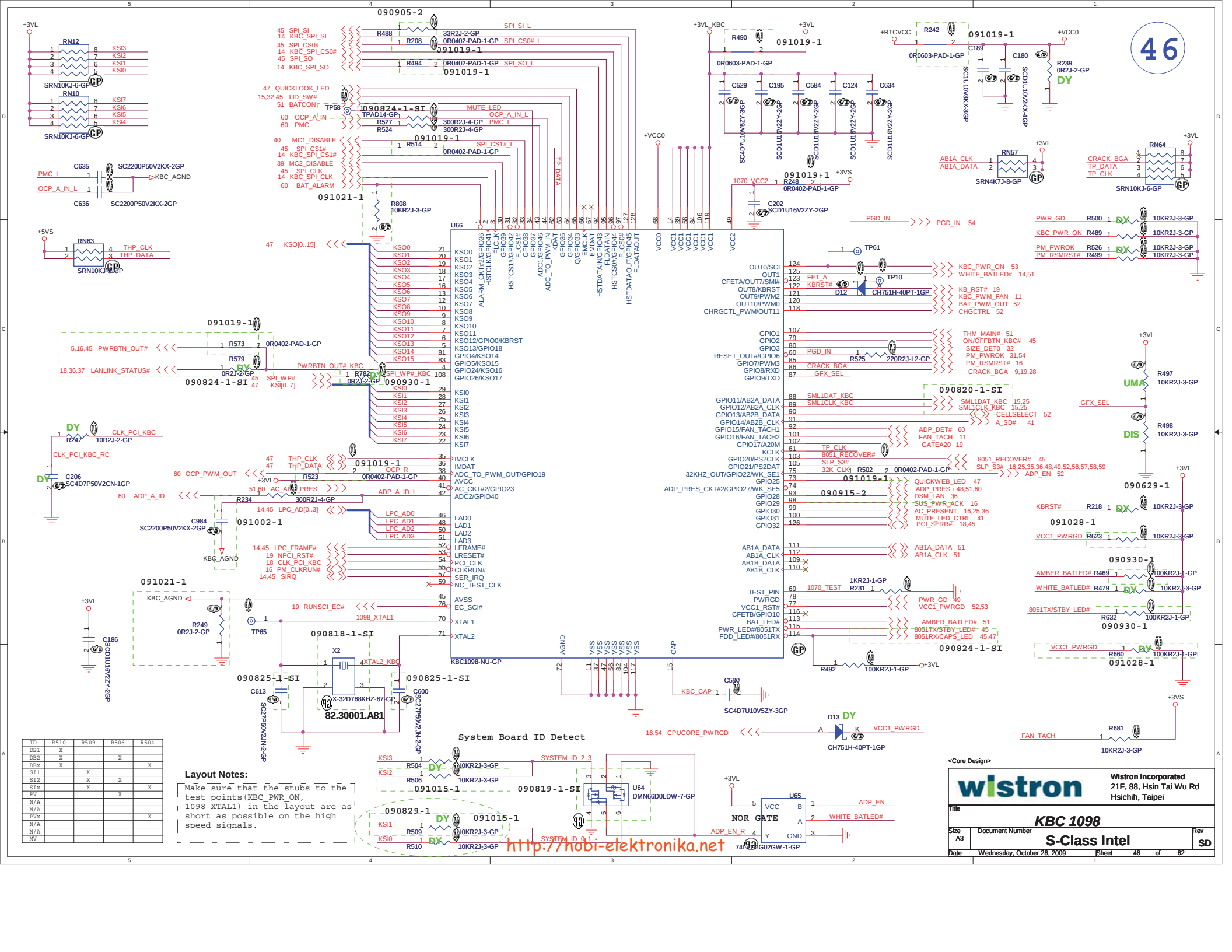
Hsichih, Taipei

Title: FWH / BTN / DEBUG CONN.

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 45 of 62


46
KBC1098-NU-GP
U66
090905-2
091019-1
091021-1
090824-1-SI
090930-1
090818-1-SI
090825-1-SI
091002-1
090915-2
090820-1-SI
090629-1
091028-1
091015-1
090819-1-SI
090829-1
82.30001.A81
System Board ID Detect
Layout Notes:
Make sure that the stubs to the test points(KBC_PWR_ON, 1098_XTAL1) in the layout are as short as possible on the high speed signals.
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Hsichih, Taipei
KBC 1098
S-Class Intel
Size A3
Rev SD
Date: Wednesday, October 28, 2009
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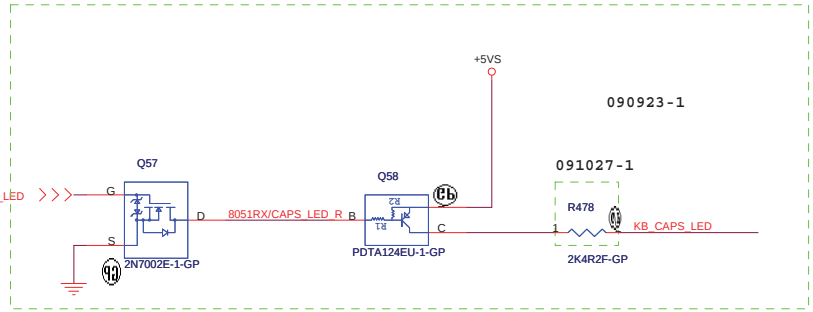
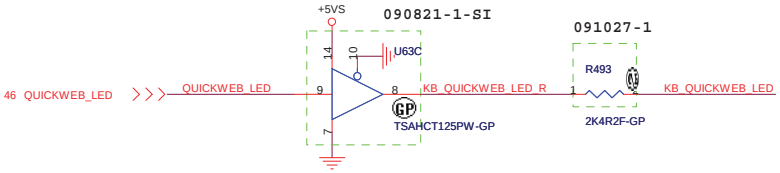
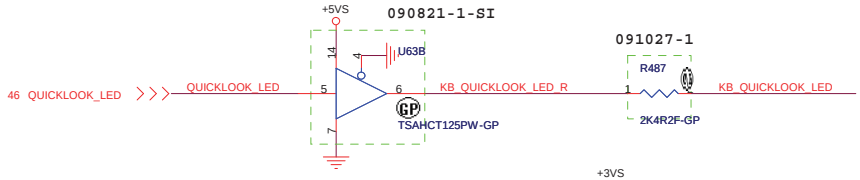
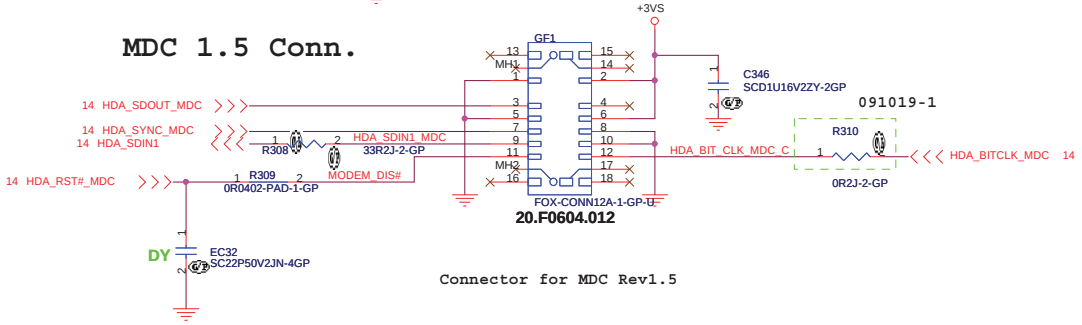




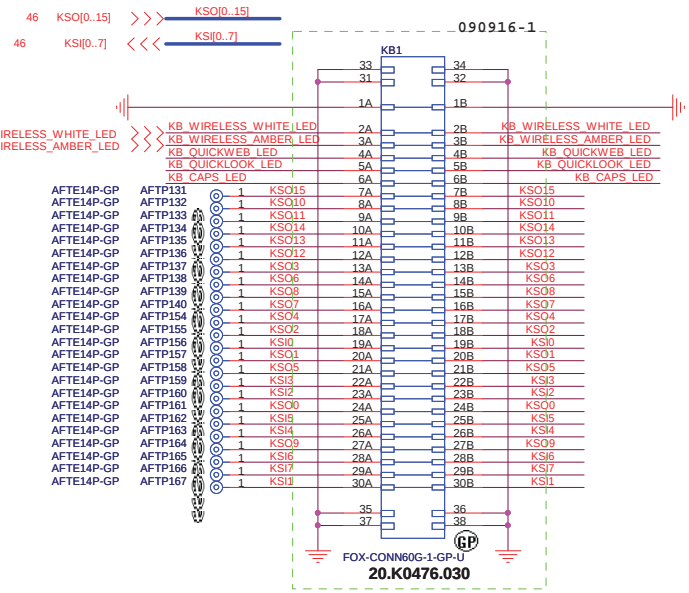


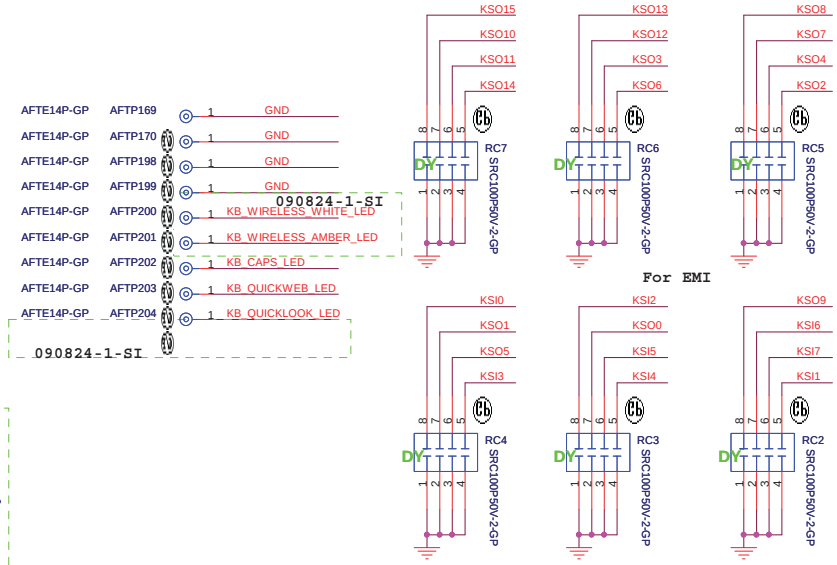
MDC 1.5 Conn.



Connector for MDC Rev1.5

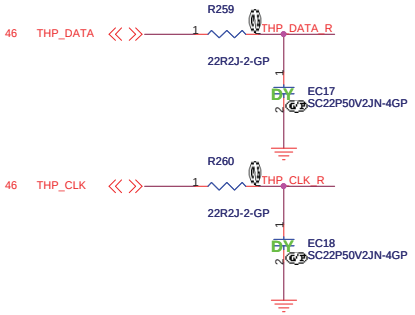
INT_KBD CONN.

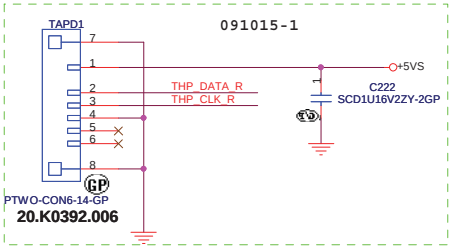


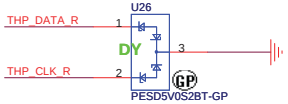


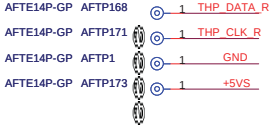
For EMI

Touch_Pad CONN.









<Core Design>

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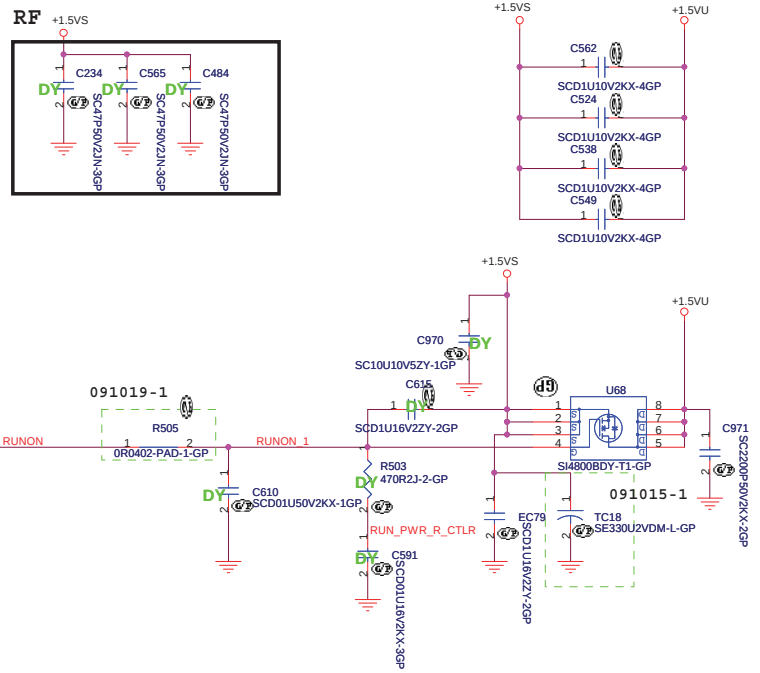
Title: MDC/KBD/ON OFF/T.P.

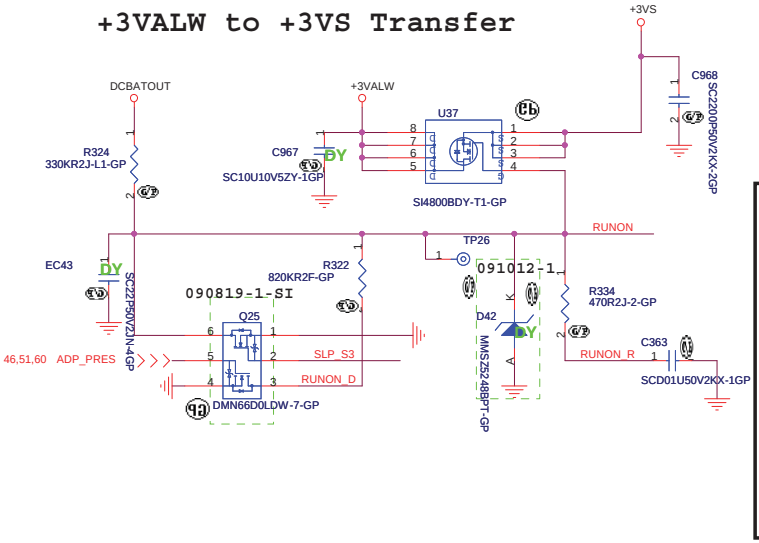
Size: A3 | Document Number: S-Class Intel | Rev: SD

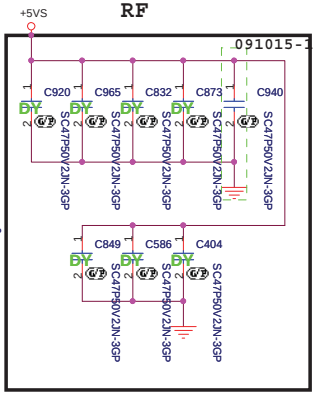
Date: Wednesday, October 28, 2009 | Sheet 47 of 62

+1.5VU to +1.5VS Transfer

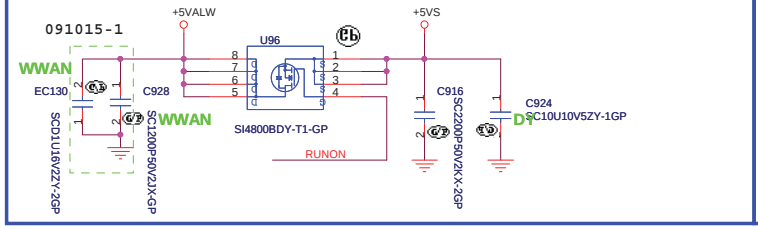


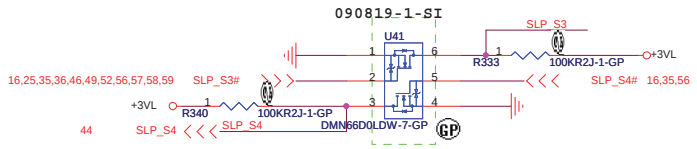
+3VALW to +3VS Transfer



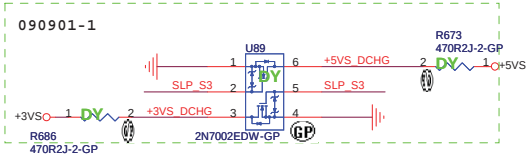


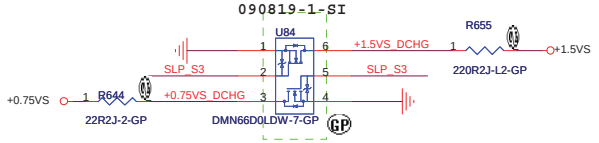
+5VALW to +5VS Transfer

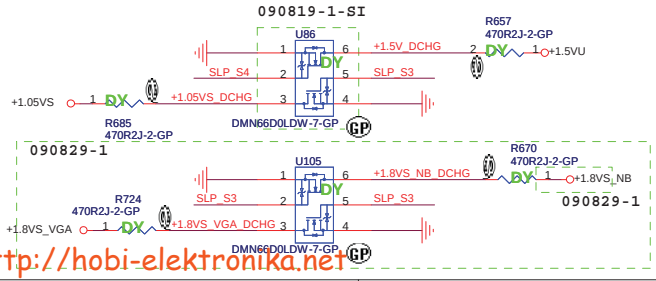




Discharge circuit-1







<Core Design>

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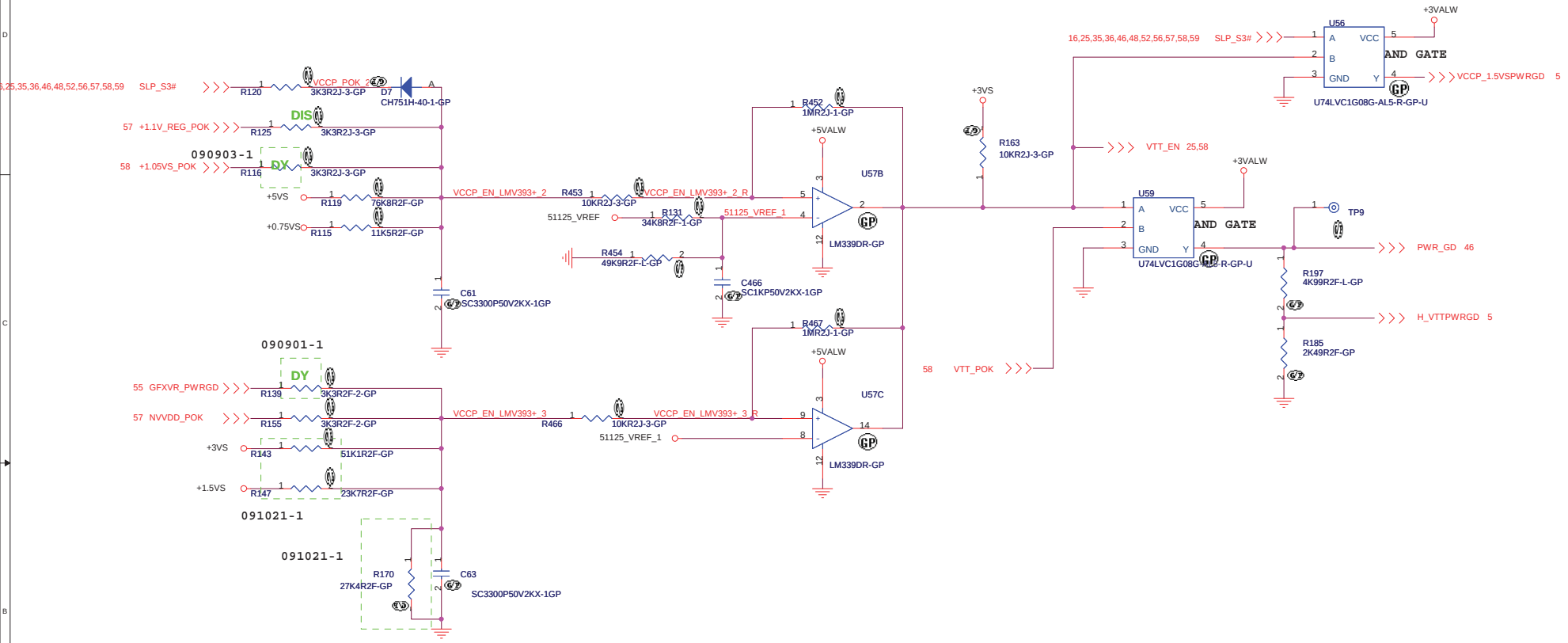
Title: DC/DC Circuit

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 48 of 62



<Core Design>

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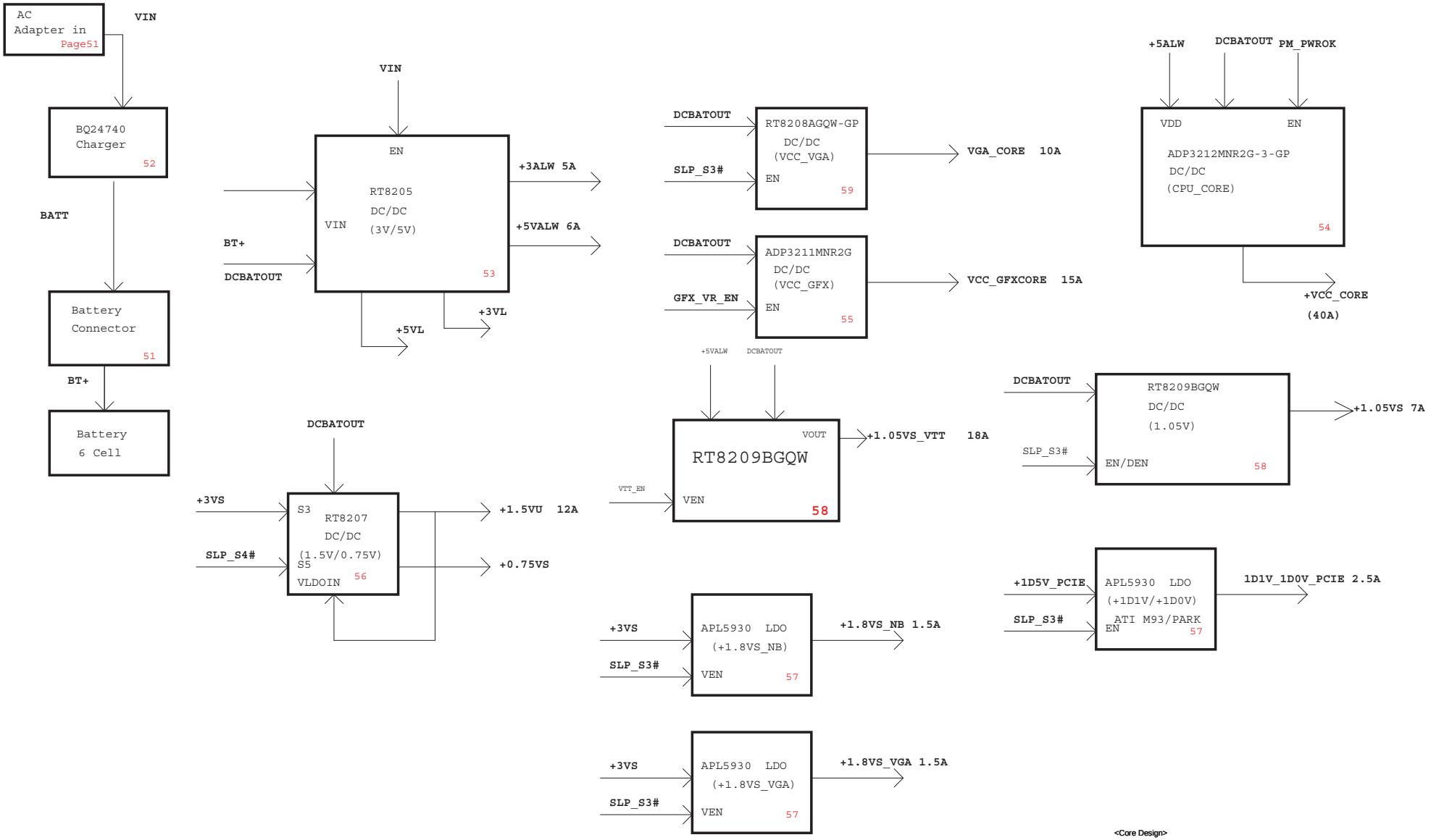
Hsichih, Taipei

Title: POK CKT

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 49 of 62

Power Block Diagram



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Title: Power Block Diagram

Size: A3 | Document Number: S-Class Intel | Rev: SD

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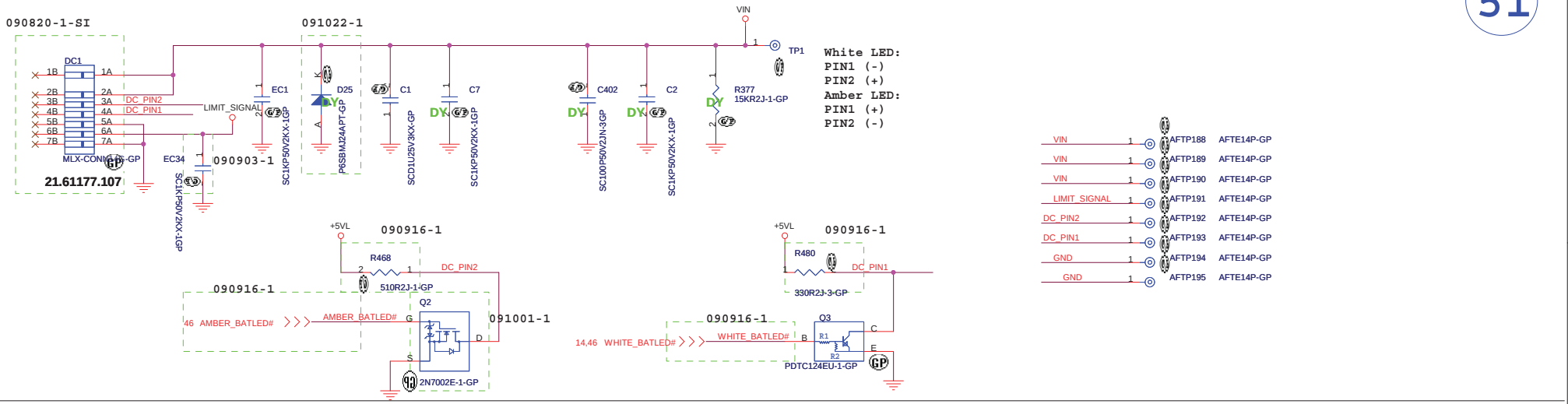
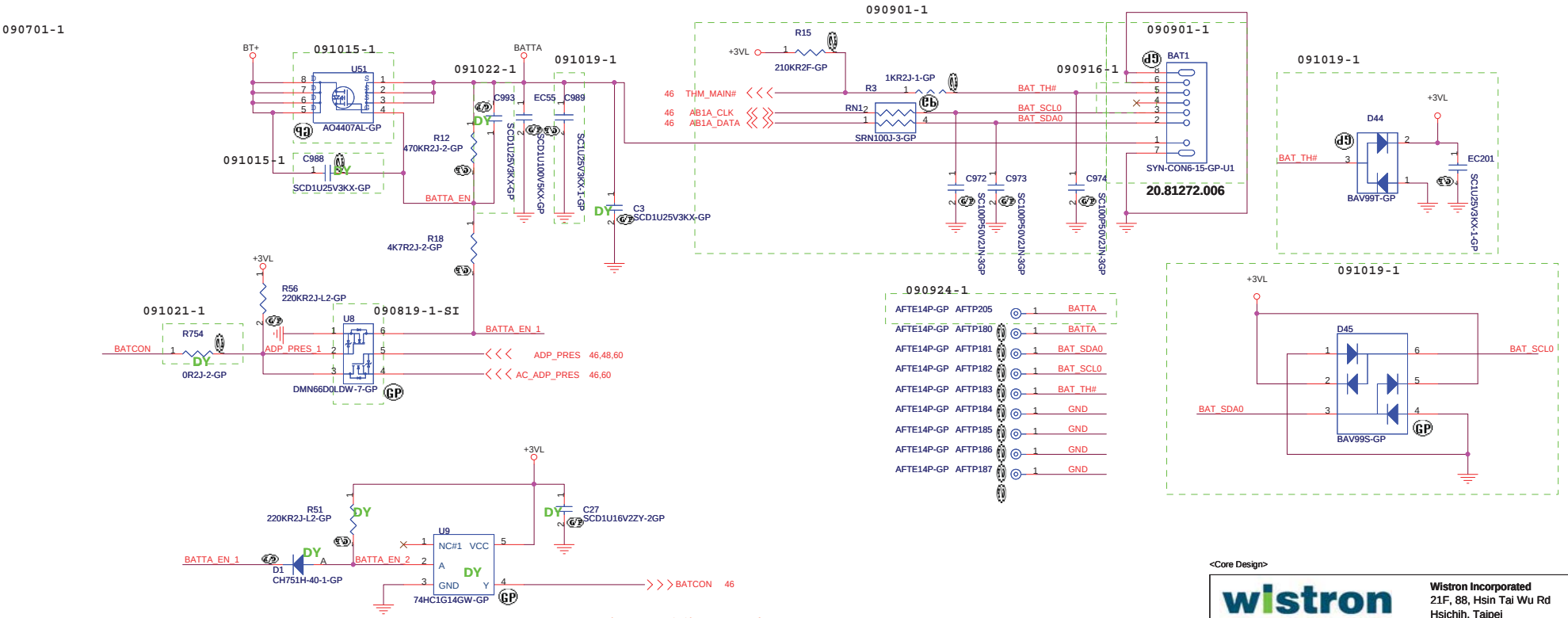
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title: DC & BATTERT CONN.

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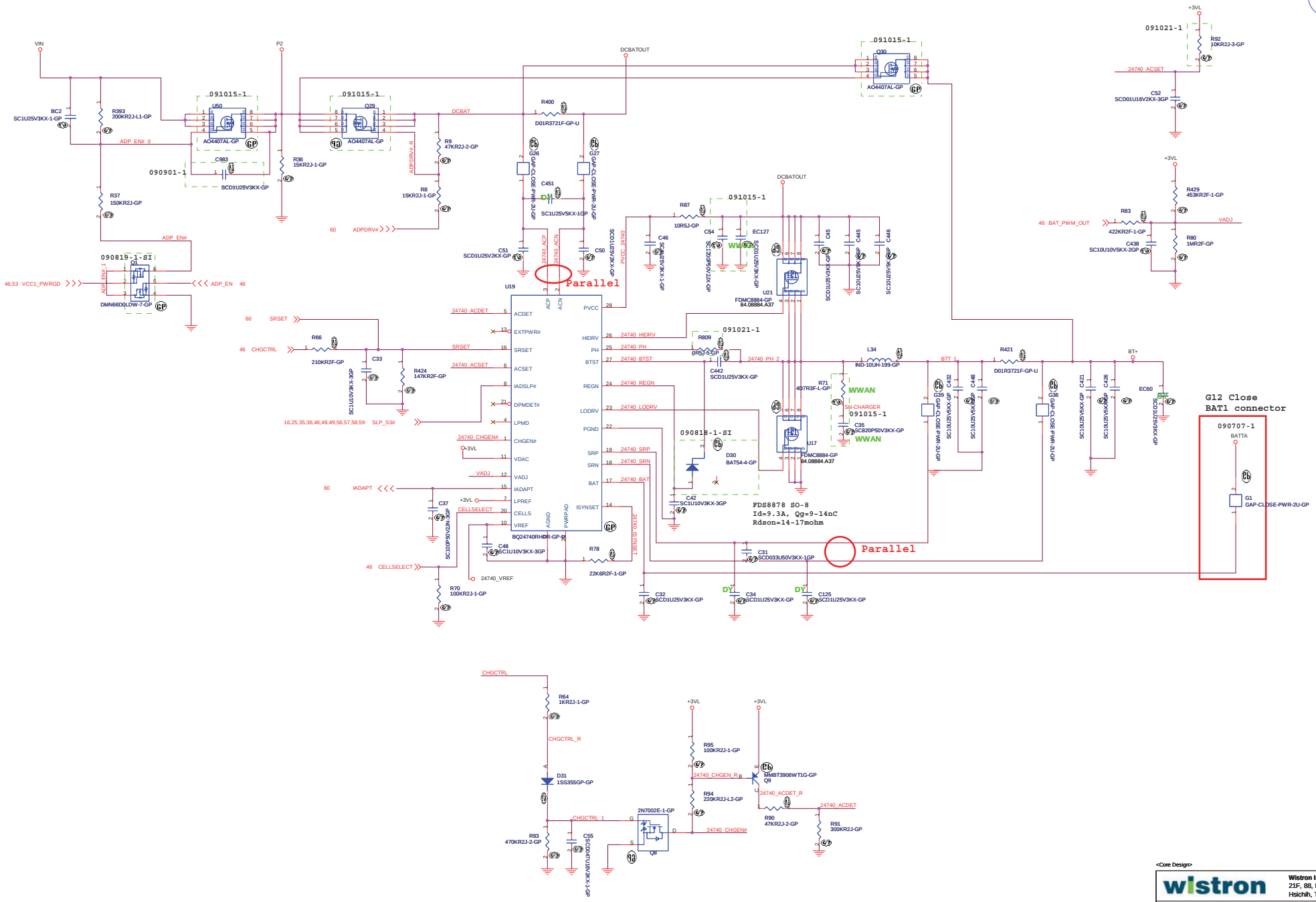
Date: Wednesday, October 28, 2009 | Sheet 51 of 62



<Core Design>
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Hsichih, Taipei
Title
CHARGER BQ24740
Size A2
Document Number
S-Class Intel
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Date: Wednesday, October 28, 2009
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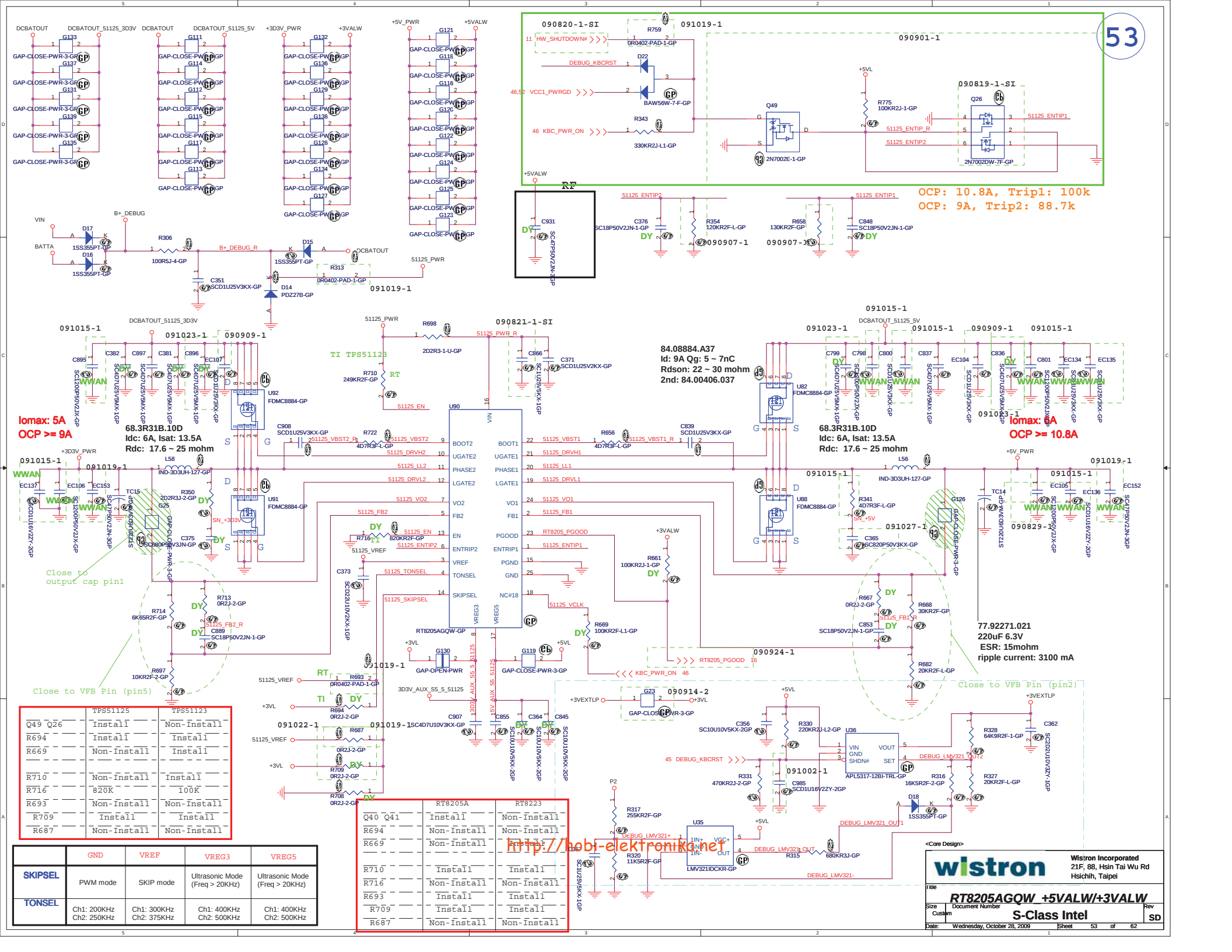
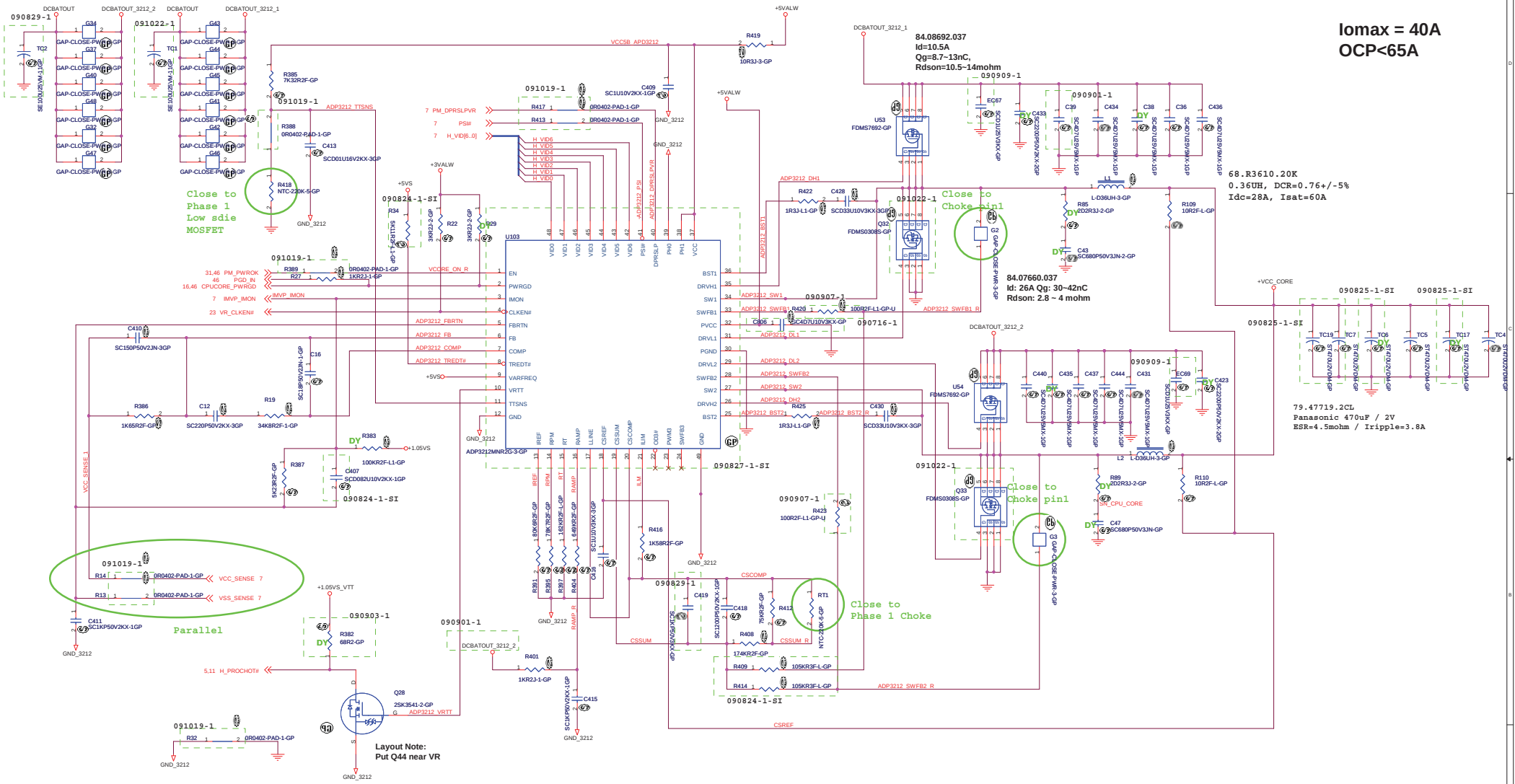


	TPS51125	TPS51123
Q49 Q26	Install	Non-Install
R694	Install	Install
R669	Non-Install	Install
R710	Non-Install	Install
R716	820K	100K
R693	Non-Install	Non-Install
R709	Install	Install
R687	Non-Install	Non-Install

	RT8205A	RT8223
Q40 Q41	Install	Non-Install
R694	Non-Install	Non-Install
R669	Non-Install	Install
R710	Install	Install
R716	Non-Install	Non-Install
R693	Install	Install
R709	Install	Install
R687	Non-Install	Non-Install

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM mode	SKIP mode	Ultrasonic Mode (Freq > 20KHz)	Ultrasonic Mode (Freq > 20KHz)
TONSEL	Ch1: 200KHz Ch2: 250KHz	Ch1: 300KHz Ch2: 375KHz	Ch1: 400KHz Ch2: 500KHz	Ch1: 400KHz Ch2: 500KHz



<Core Design>
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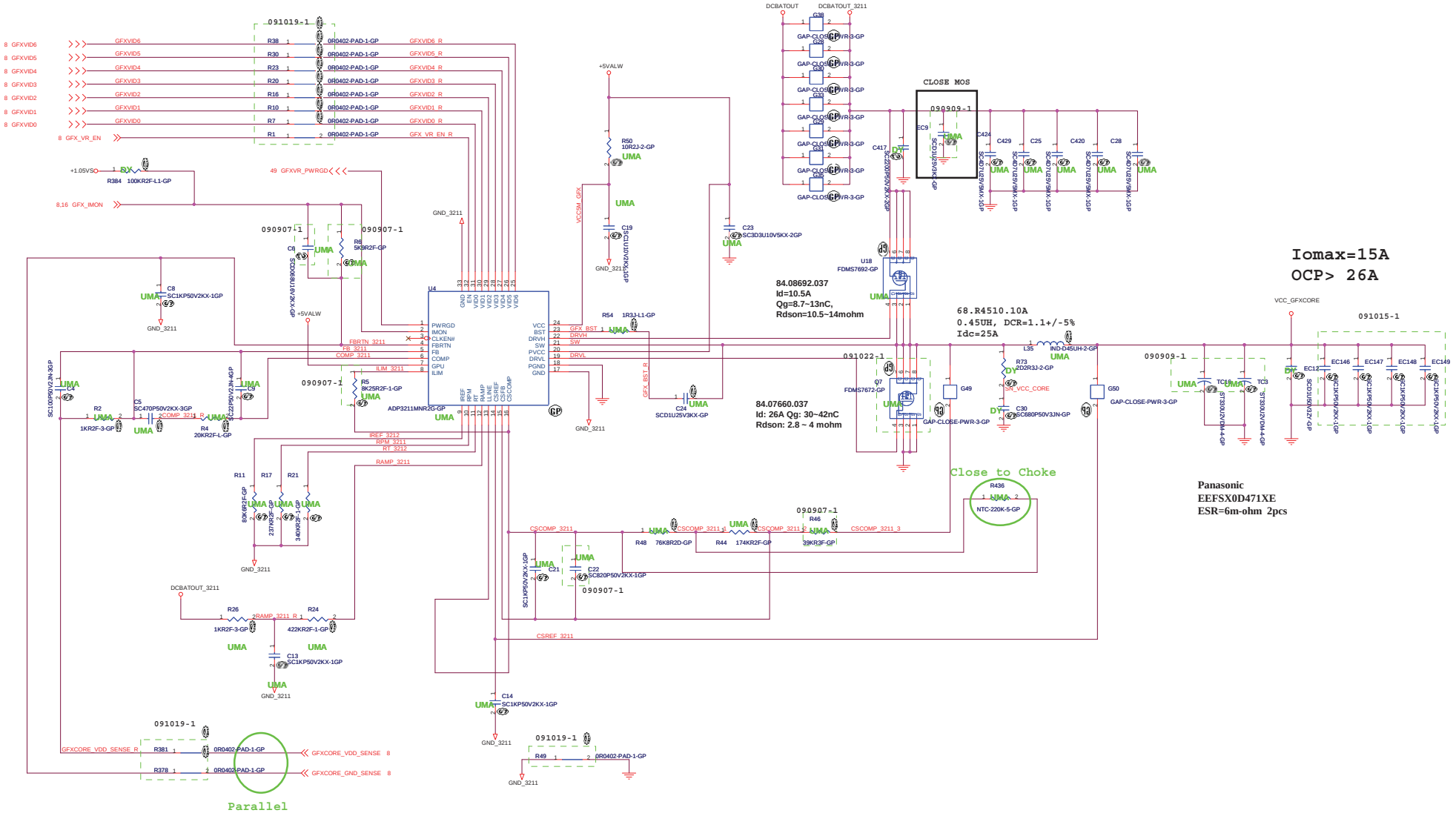
Title: ADP3212MNR2G_CPU CORE

Size: A2 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 54 of 62



<Core Design>
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Title: ADP3211MNR2G_+VCC_GFX_CORE

Size	Document Number	Rev
A2	S-Class Intel	SD

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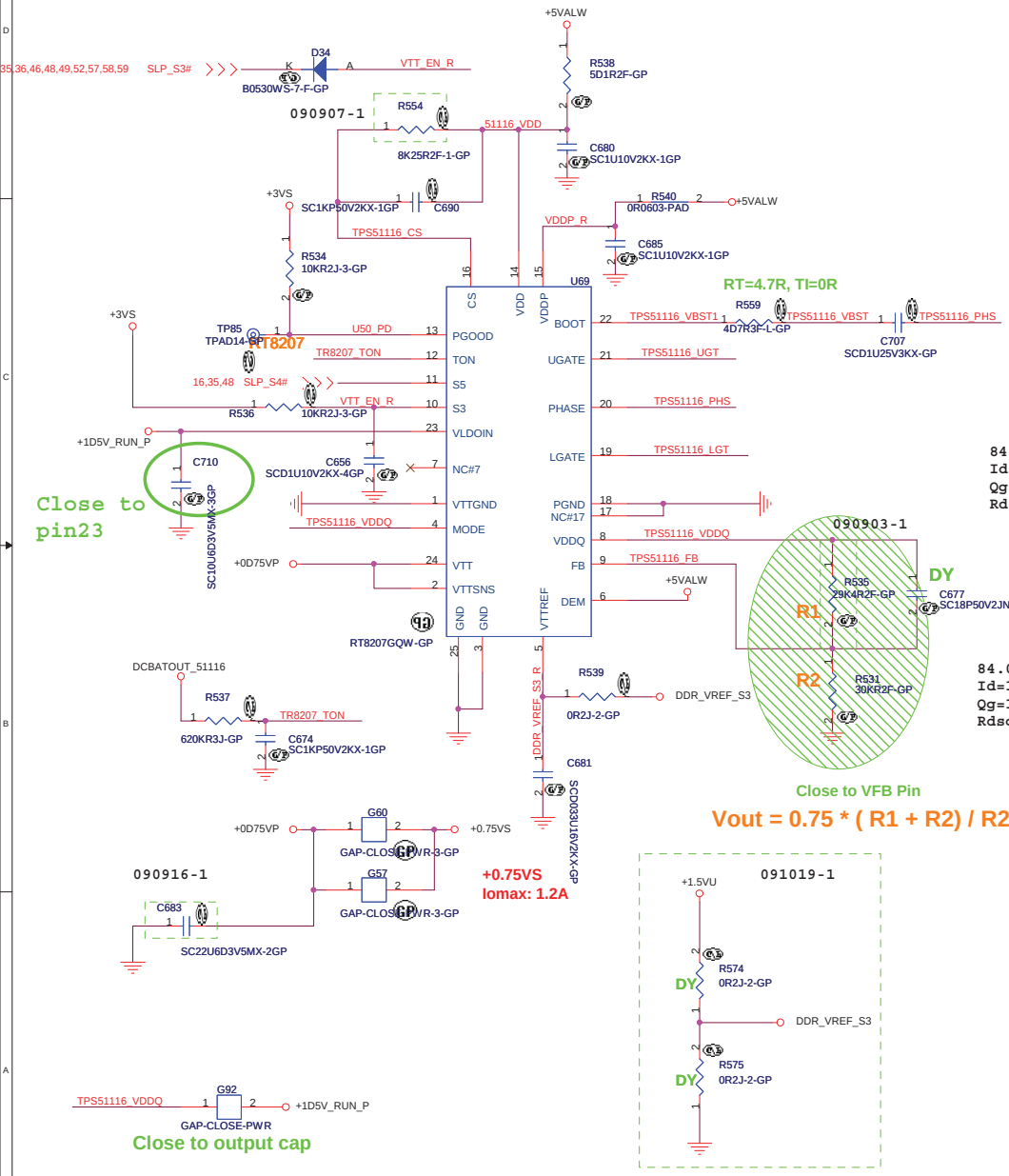
RT8207 for 1D5V and 0D75V



<Core Design>

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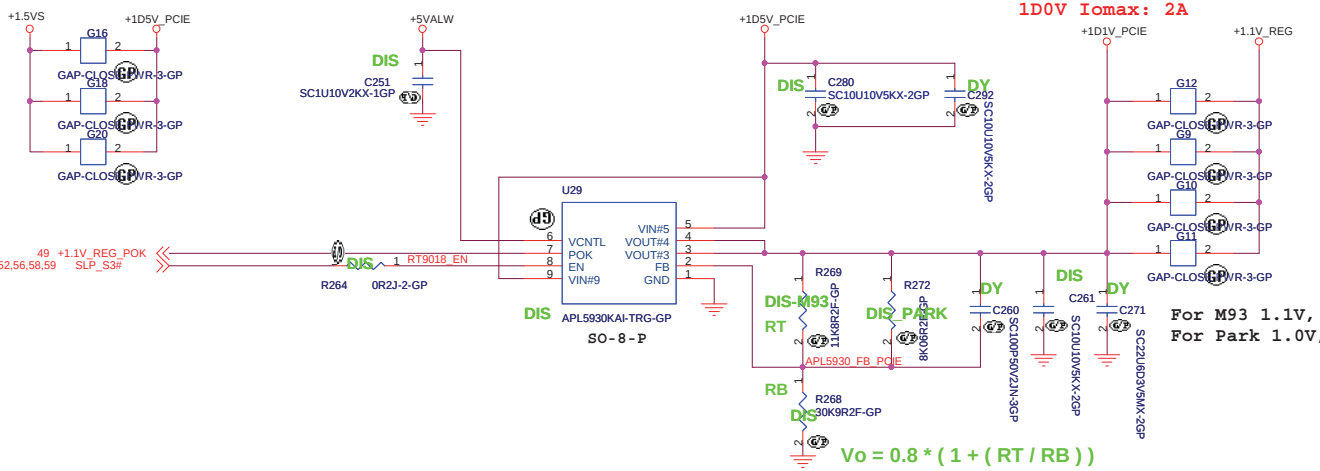
Title: RT8207GQW +1.5VU / +0.75VS

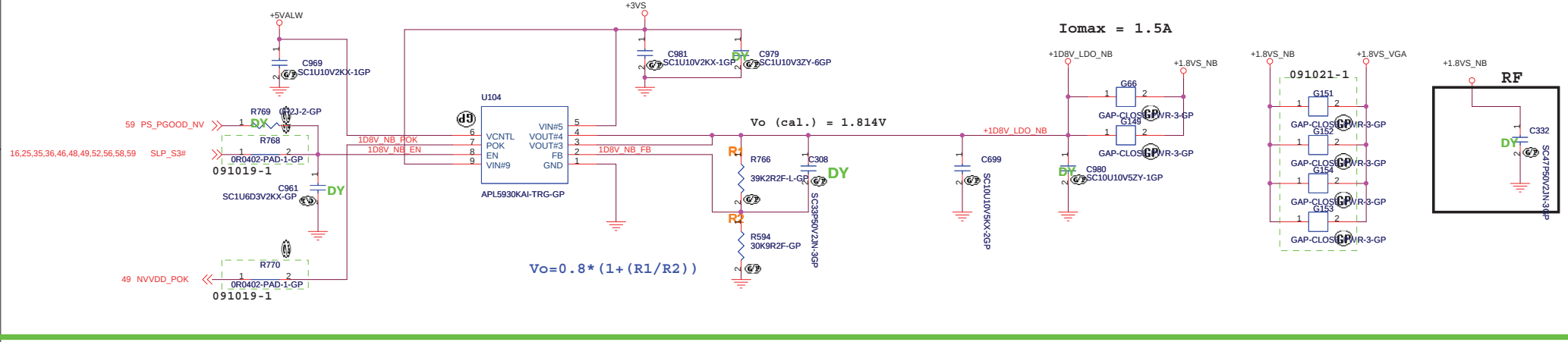
Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 56 of 62

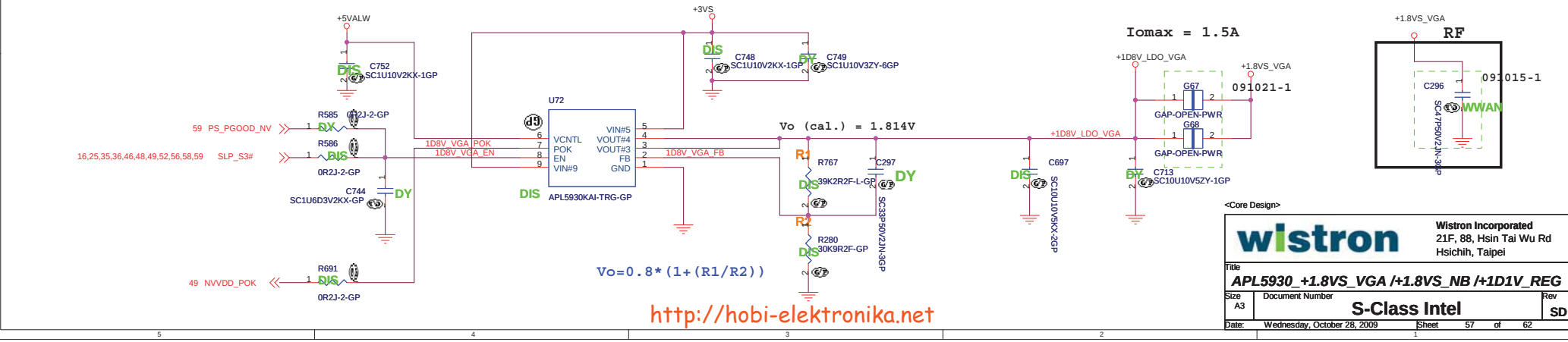
1D1V Iomax: 2.5A
1D0V Iomax: 2A



For M93 1.1V, RT=11.8K, Vo(cal.)=1.105V
For Park 1.0V, RT=8.06K, Vo(cal.)=1.008V



Iomax = 1.5A



Iomax = 1.5A

<Core Design>

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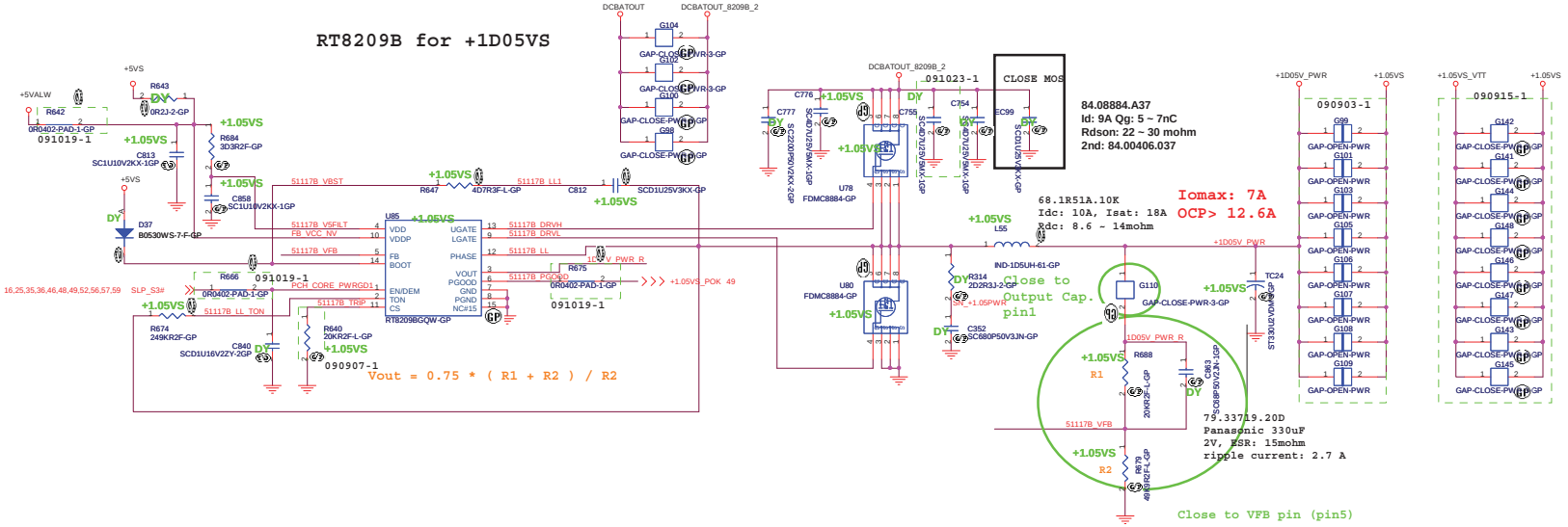
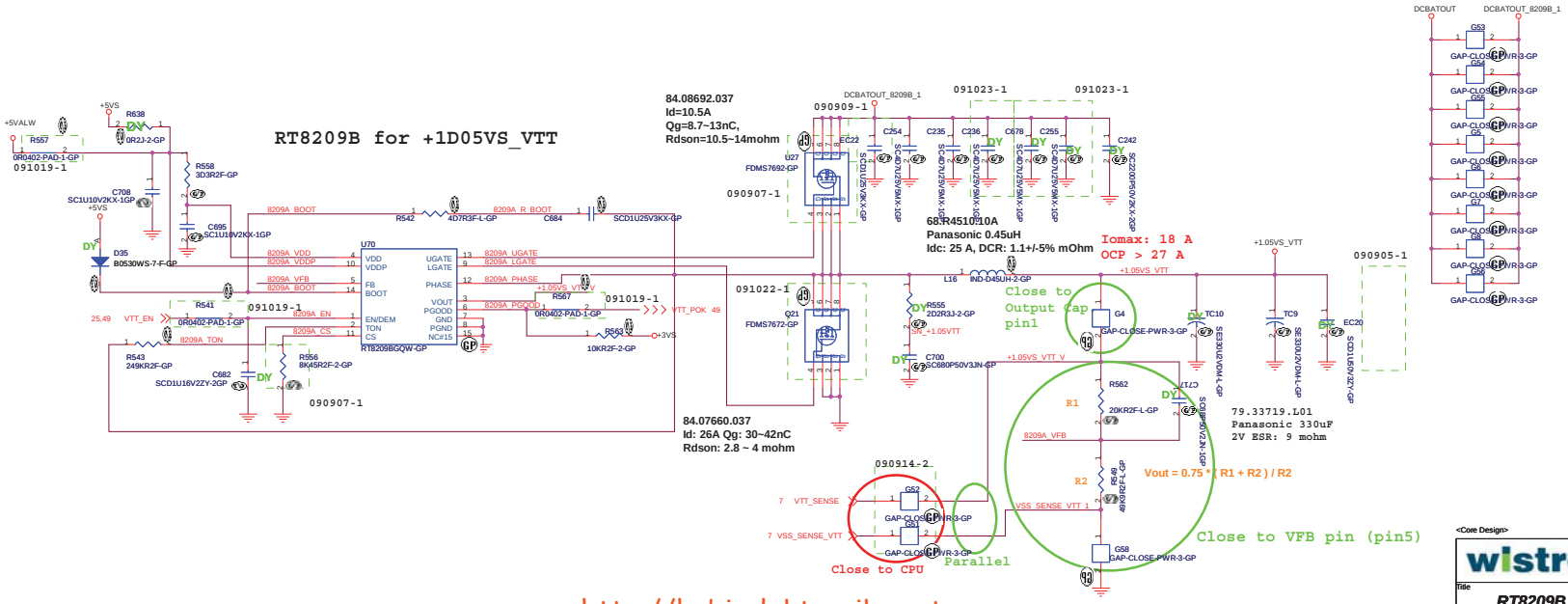
Title: APL5930_+1.8VS_VGA /+1.8VS_NB /+1D1V_REG

Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 Sheet 57 of 62





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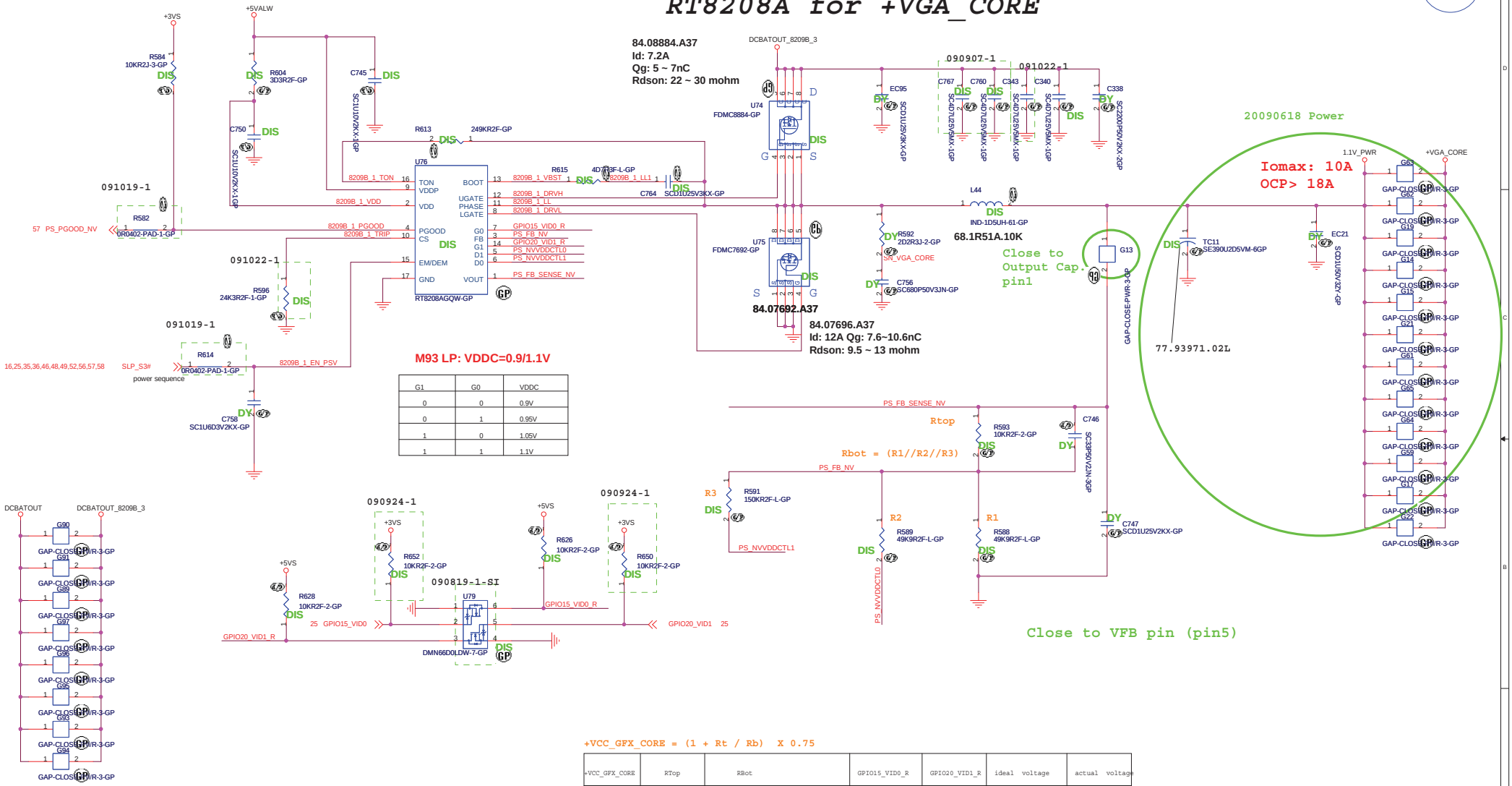
Title: RT8209B +1.05VS_VTT /+1.05VS

Size: A2 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 58 of 62

RT8208A for +VGA_CORE



G1	G0	VDDC
0	0	0.9V
0	1	0.95V
1	0	1.05V
1	1	1.1V

+VCC_GFX_CORE = (1 + Rt / Rb) X 0.75

+VCC_GFX_CORE	RTop	RBot	GPIO15_VID0_R	GPIO20_VID1_R	ideal voltage	actual voltage
0.9v	10k	R1 49.9k	LOW	LOW	0.9003	
0.95v	10k	R1 R2 49.9k // 49.9k	LOW	HIGH	0.9493	
1.05v	10k	R1 R3 49.9k // 150k	HIGH	LOW	1.0506	
1.1v	10k	R1 R2 R3 49.9k // 49.9k // 150k	HIGH	HIGH	1.0997	

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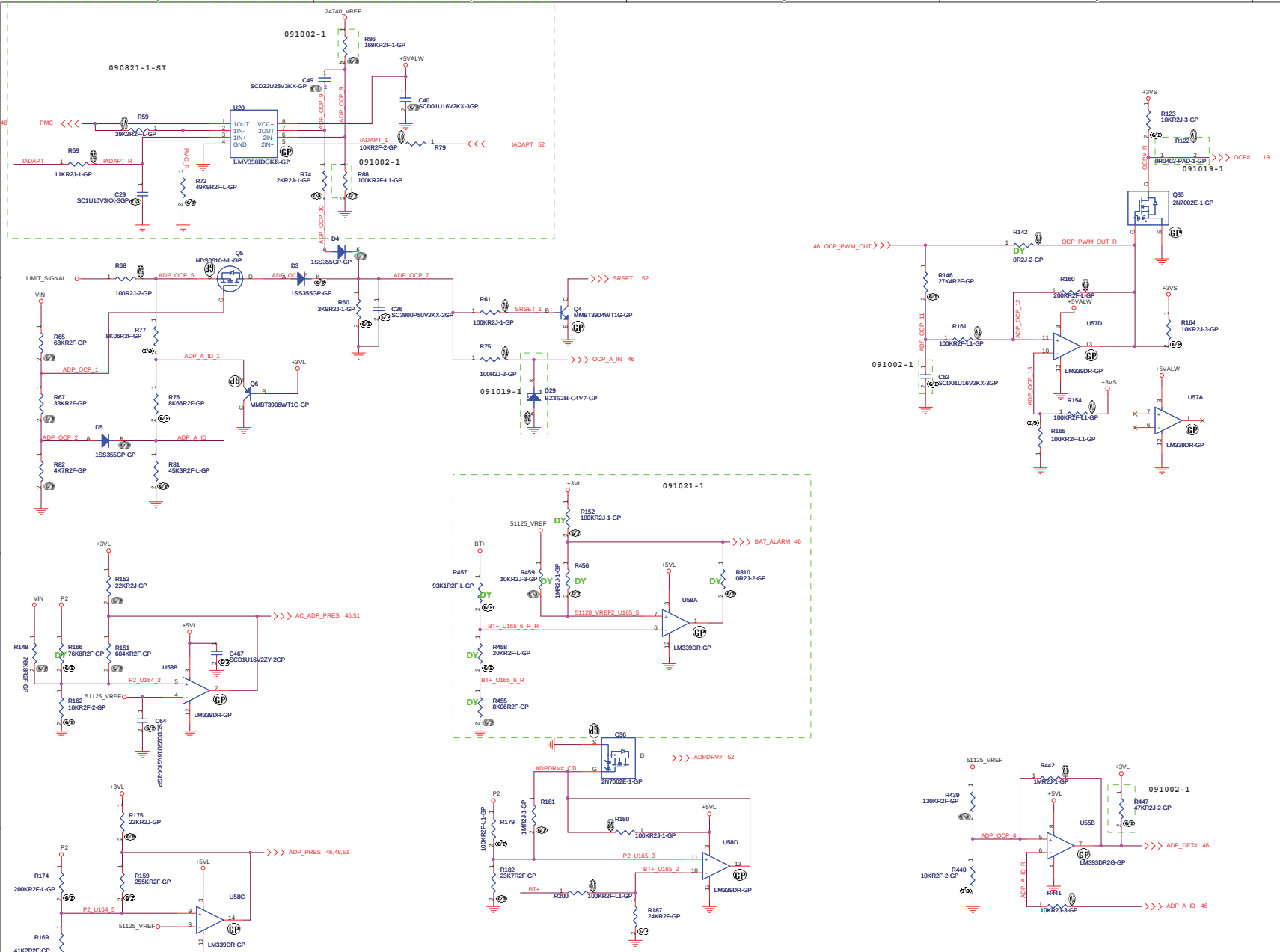
Title: RT8208AGQW_+VGA_CORE

Size: Custom | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 59 of 62



<Core Design>

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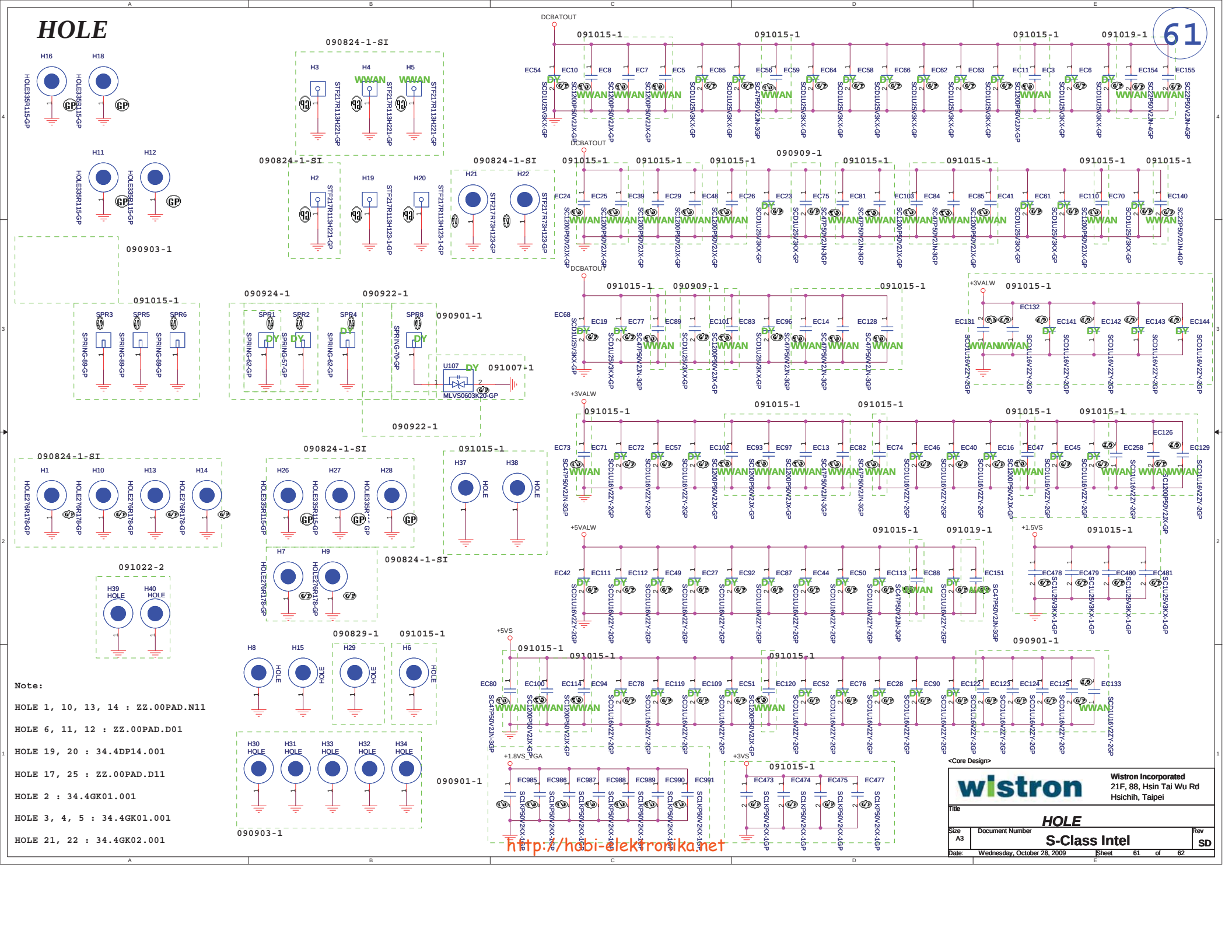
Title: ADP OCP

Size: A2 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 60 of 82


HOLE
61
Note:
HOLE 1, 10, 13, 14 : ZZ.00PAD.N11
HOLE 6, 11, 12 : ZZ.00PAD.D01
HOLE 19, 20 : 34.4DP14.001
HOLE 17, 25 : ZZ.00PAD.D11
HOLE 2 : 34.4GK01.001
HOLE 3, 4, 5 : 34.4GK02.001
HOLE 21, 22 : 34.4GK02.001
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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
HOLE
Size A3
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Date: Wednesday, October 28, 2009
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Title

Change Notes List

Size	Document Number	Rev
A3	S-Class Intel	SD

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