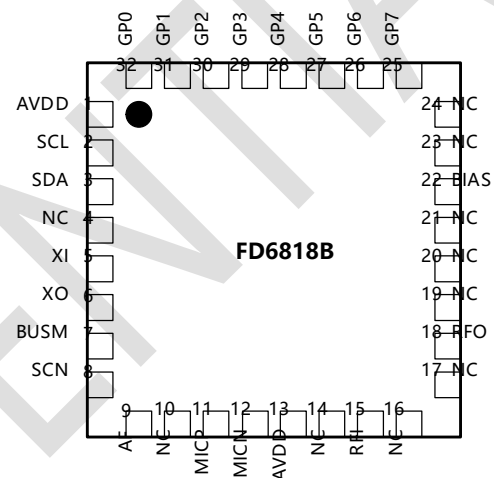


## Analog Two Way Radio Transceiver

FD6818B is a highly integrated single chip transceiver for digital and analog walkie-talkie applications performing the functions of VHF/UHF band amplification and filtering, quadrature down conversion, local oscillator generation, baseband gain and filtering, automatic gain control (AGC) and DC offset correction, sub-audio and audio processing.

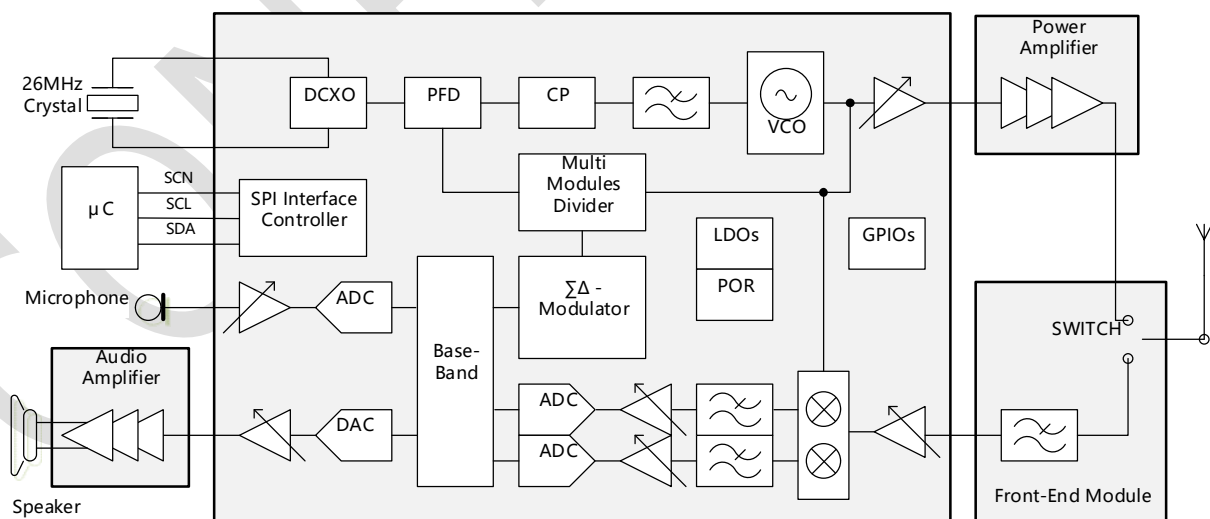
This device is designed to manage very low signal-to-noise ratio carriers, in the presence of multiple unwanted channels and adjacent channel interference. This scenario is particular to some applications of the Walkie-Talkie down-link set-ups. The transceiver IC contains an LNA, integrated VCOs and synthesizers, an RF VGA, quadrature mixers, variable gain baseband amplifiers, variable baseband filters, ADCs and digital low-IF converter, and power drivers.

support multiple standards and markets. Controlled via a serial interface (2 or 3-wire) the Family Radio Processor operates from a 2.4V to 3.6V supply and is available in 32-pin QFN5x5 package.



FD6818B Top View

By using the FD6818B one global radio design can



FD6818B Functional Block Diagram

## FEATURES

- ✔ World wide band: 16 MHz ~ 560 MHz, 740 MHz ~1120 MHz
- ✔ 12.5/20/25 kHz channel spacing
- ✔ On chip 8 dBm RF PA
- ✔ 2.4 V to 3.6 V power supply
- ✔ CTCSS generator and decoder (two parallel frequency detector)
- ✔ DCS (23/24 bit programmable) generator and decoder
- ✔ Selectable pre-emphasis and de-emphasis
- ✔ Selectable frequency inversion scrambler
- ✔ Selectable voice compandor
- ✔ Microphone and Discriminator Analogue Inputs baseband process mode
- ✔ DTMF/SELCALL (up to 16 tones) encoder and decoder
- ✔ FSK encoder and decoder (DTMF/SELCALL and FSK can receive simultaneously)
- ✔ Tx limiter and splatter filter (programmable)
- ✔ Audio call (single or dual) tone generator
- ✔ Digital and analog gain adjustment
- ✔ RF Signal strength measurement and signal quality measurement
- ✔ Voice activated switch (VOX) and time-out timer
- ✔ Programmable PA Bias output from 1.2V to 2.8V
- ✔ Frequency scan function
- ✔ 3 or 8 GPIOs
- ✔ Support 12 MHz~13 MHz, 18 MHz~20 MHz and 24 MHz~26 MHz XTAL
- ✔ 32-pin QFN5x5 package

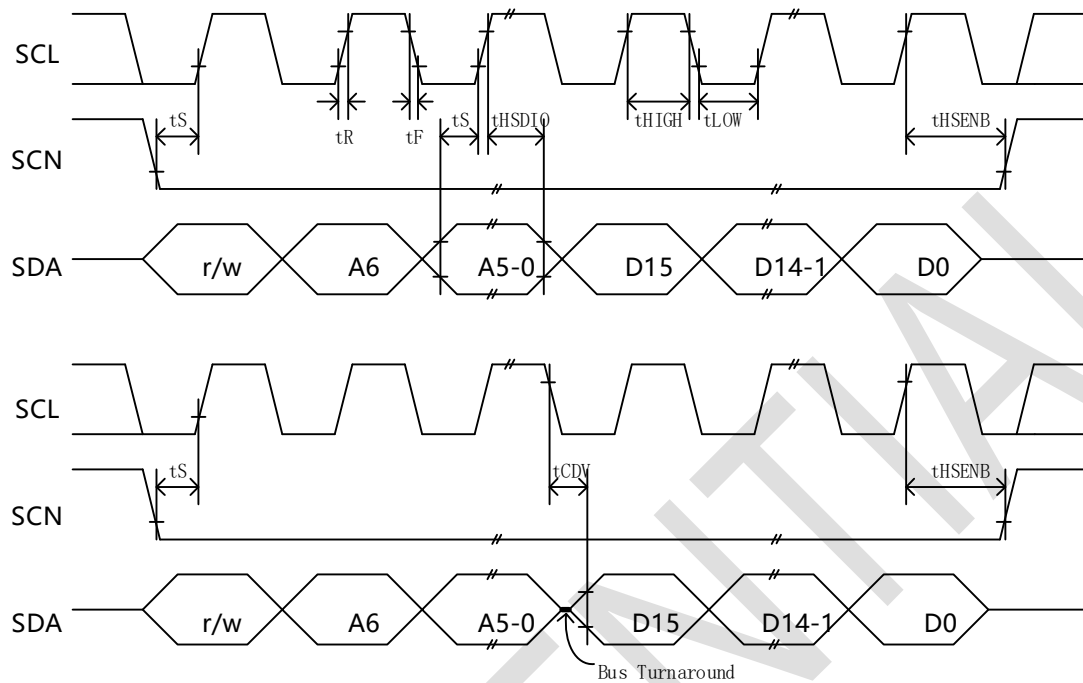
## APPLICATIONS

- ✔ Walkie-Talkies / FRS / PMR / GMRS

- ✓ DMR / dPMR / PDT Transceiver
- ✓ Toys / Baby Monitor
- ✓ Smart Home
- ✓ Remote Data Transmission
- ✓ Short Range Devices

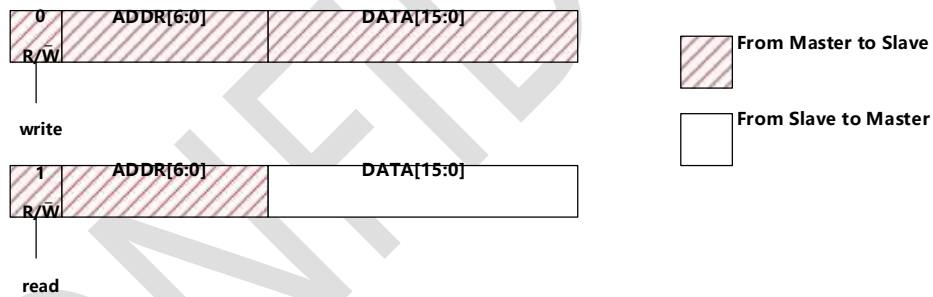
### 3-WIRE CONTROL INTERFACE CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.
SCL Frequency	fSCL	0 MHz	—	8 MHz
SCL High Time	tHIGH	25 ns	—	—
SCL Low Time	tLOW	25 ns	—	—
SDA Input, SCN to SCL↑ Setup	tS	20 ns	—	—
SDA Input to SCL↑ Hold	tHSDA	10 ns	—	—
SCN Input to SCL↓ Hold	tHSCN	10 ns	—	—
SCL↓ to SDA Output Valid	tCDV	2 ns	—	25 ns
SCL, SCN, SDA, Rise/Fall Time	tR,tF	—	—	10 ns



3-wire interface timing

#### Format

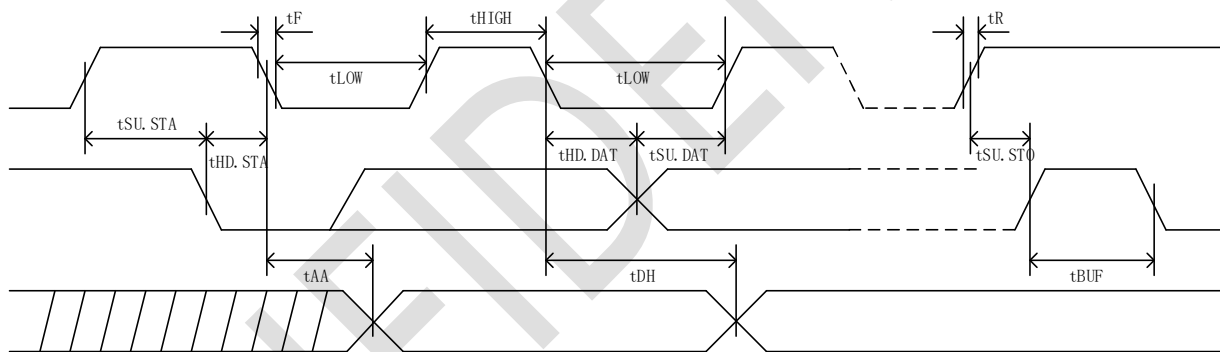


## 2-WIRE CONTROL INTERFACE CHARACTERISTICS

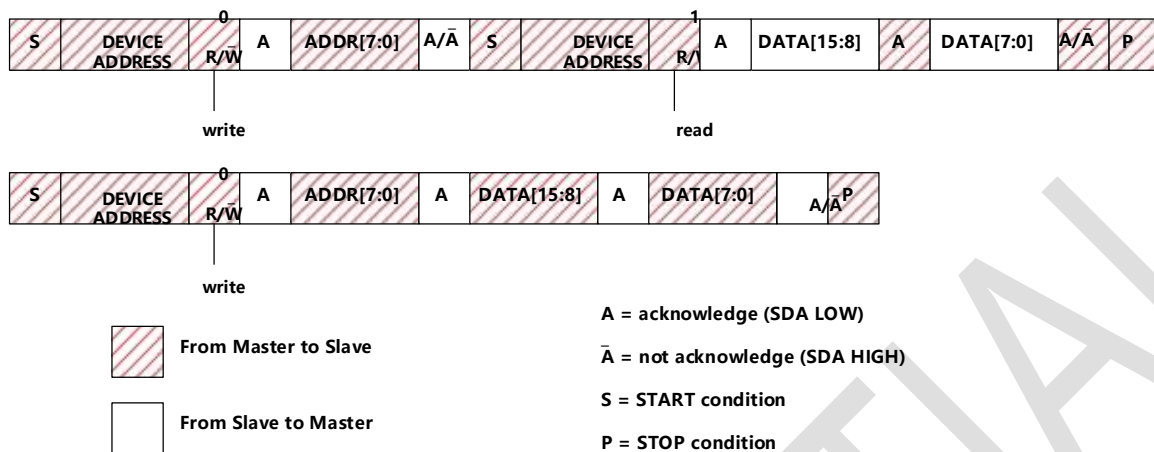
Parameter	Symbol	Min	Max	Unit
Clock Frequency, SCL	fSCL		400	kHz
Clock Pulse Width Low	tLOW	1.2		$\mu$ s
Clock Pulse Width High	tHIGH	0.6		$\mu$ s
Clock Low to Data Out Valid	tAA	0.1	0.9	$\mu$ s

## FD6818B

Time the bus must be free before a new transmission can start.	tBUF	1.2		$\mu\text{s}$
Start Hold Time	tHD.STA	0.6		$\mu\text{s}$
Start Setup Time	tSU.STA	0.6		$\mu\text{s}$
Data In Hold Time	tHD.DAT	100		ns
Data In Setup Time	tSU.DAT	100		ns
Inputs Rise Time	tR		0.3	$\mu\text{s}$
Inputs Fall Time	tF		300	ns
Stop Setup Time	tSU.STO	0.6		$\mu\text{s}$
Data Out Hold Time	tDH	100		ns
Write Cycle Time	tWR	5		ms



Format (Device Address = '0101110' when SCN is high(or no SCN pin), or Device Address = '1110001' when SCN is low):



## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage from battery or LDO	AVDD	2.6	—	3.6	V
Ambient Temperature	Tamb	-25	27	+85	°C

## ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Min	Typ	Max	Unit
Ambient Temperature	Tamb	-40	—	+90	°C
Input Current	IIN	-40	—	+90	
Input Voltage	VIN	-10	—	+10	
LNA Input Level	VIna	-0.3	—	3.3	

**DC CHARACTERISTICS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD	-0.3	—	+3.6	V
I/O pin voltage	VIO	-0.3	—	VDD+0.3	V
Storage Temperature	TS	-20	25	85	°C

**POWER CONSUMPTION SPECIFICATION (AVDD = 3.3 V, TA = -25 TO 85°C)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Current (RX @-120dBm RF signal input)	IRX	—	40	—	mA
Supply Current (TX @maximum power output)	ITX	—	30	—	mA
Power Down Current	IPD	—	200	—	μA

**RECEIVER CHARACTERISTICS (446.00625MHZ)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Modulation Bandwidth	MDBW	1	2x3			kHz
Sensitivity	SENS	1, 2, 3		-125		dBm
Adjacent Channel Selectivity	ACS	1, 4		68		dB
Blocking	BLK	1, 5		85		dB
Co-channel Rejection	CCR	1		-7		dB
Inter-modulation	IMD	1		65		dB
SINAD	ASINAD	3, 6		57		dB
AF distortion	ADIST	3, 6		0.1		%
AF response	ARES	1		-3~+3		dB

Test Condition:

1. According to the standard "ETSI EN 300 086-1 V1.4.1 (2010-6)" , 12.5kHz mode
2. 12 dB SINAD
3. 1kHz sine, 1.5kHz deviation
4. 1st adjacent channel (12.5kHz)
5. Frequency offset > 1MHz
6. -47dBm input power

## TRANSMITTER CHARACTERISTICS (446.00625MHZ)

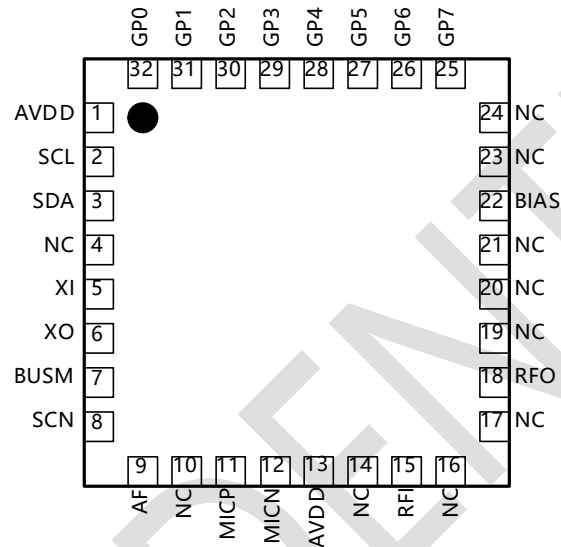
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Power	POUT				8	dBm
Modulation Limiting	MDLMT	1			2.5	kHz
Adjacent Channel Power Rejection	ACPR 1 <sup>st</sup>	1, 3, 6		65		dBc
Alternate Channel Power Rejection	ACPR 2 <sup>nd</sup>	1, 4, 6		73		dBc
Microphone Sensitivity	MICSENS	5	10			mV
SINAD	TSINAD	2	47			dB
AF response	TARES		-3~+3			dB
Distortion	TDIST	2	0.4			%

Test Condition:

1. According to the standard "ETSI EN 300 086-1 V1.4.1 (2010-6)" , 12.5kHz mode
2. 1.5kHz deviation
3. +/-12.5kHz frequency offset
4. +/-25kHz frequency offset
5. At sensitivity level
6. Maximum power output



## PIN ASSIGNMENT &amp; DEFINITION



FD6818B Top View

PIN#	Signal Name	Type	Description
1	AVDD	PWR	Power supply.
2	SCL	IP+PU	The 2 or 3-wire serial clock input from the MCU - there is internal pull-up on this input.
3	SDA	BI+PU	The 2 or 3-wire serial data between the chip and the MCU - there is internal pull-up on this input.
4	NC	NC	No connection.
5	XI	IP	Crystal oscillator input.
6	XO	OP	Crystal oscillator output.
7	BUSM	IP	Bus Mode Selection. 'HIGH' : 3-wire; 'LOW' : 2-wire

8	SCN	IP+PU	The 3-wire chip select input from the MCU - there is internal pull-up on this input.
9	AF	OP	Audio Frequency signal output to speaker.
10	NC	NC	No connection.
11	MICP	IP	Microphone input, negative.
12	MICN	IP	Microphone output, positive.
13	AVDD	PWR	Power supply.
14	NC	NC	No connection.
15	RFI	IP	RF signal input.
16	NC	NC	No connection.
17	NC	NC	No connection.
18	RFO	OP	RF signal output.
19	NC	NC	No connection.
20	NC	NC	No connection.
21	NC	NC	No connection.
22	BIAS	OP	Bias supply for PA or others.
23	NC	NC	No connection.
24	NC	NC	No connection.
25	GP7	BI+PD	General purpose input/output - there is internal pull-down on this bi-port.
26	GP6	BI+PD	General purpose input/output - there is internal pull-down on this bi-port.
27	GP5	BI+PD	General purpose input/output - there is internal pull-down on this bi-port.
28	GP4	BI+PD	General purpose input/output - there is internal pull-down on this bi-port.

29	GP3	BI+PD	General purpose input/output - there is internal pull-down on this bi-port.
30	GP2	BI+PD	General purpose input/output - there is internal pull-down on this bi-port.
31	GP1	BI+PD	General purpose input/output - there is internal pull-down on this bi-port.
32	GP0	BI+PD	General purpose input/output - there is internal pull-down on this bi-port.

**Notes:** IP = Input (+ PU/PD = internal pullup/pulldown resistor)

OP = Output

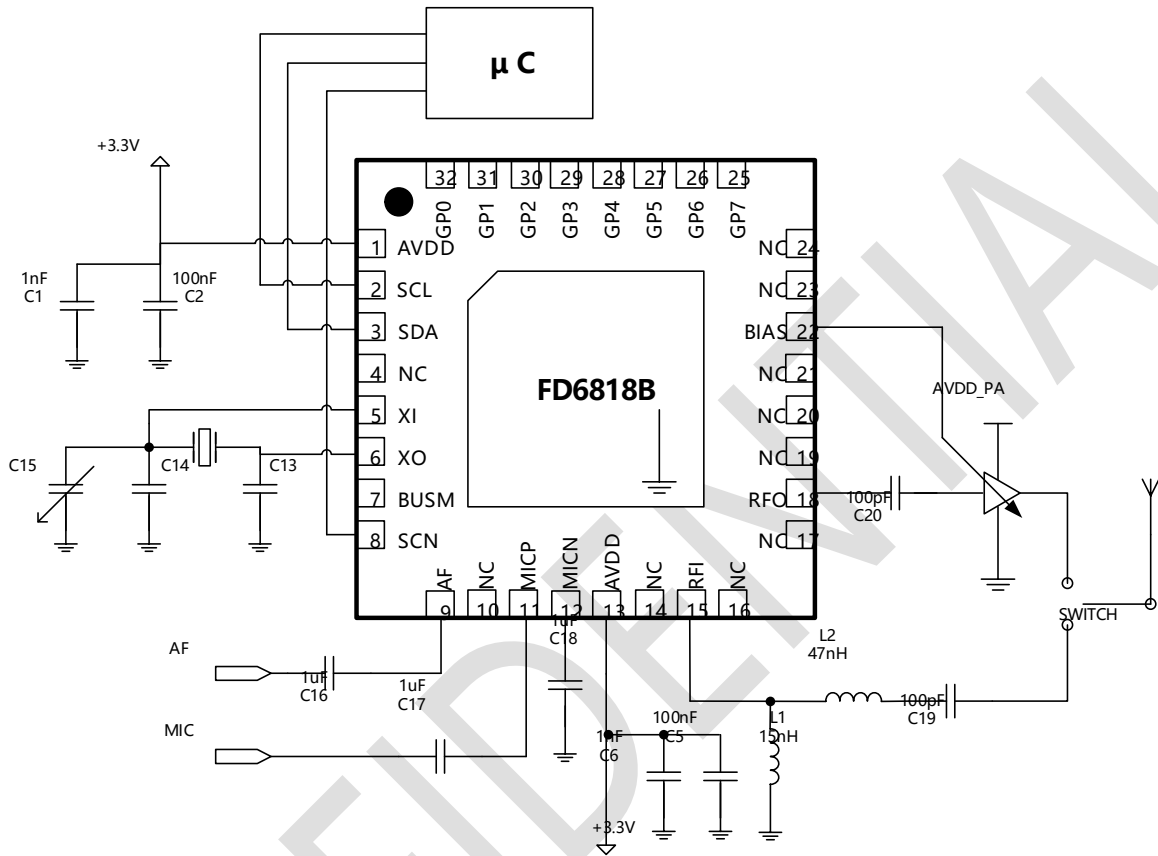
BI = Bidirectional

PWR = Power Connection

GD = Ground

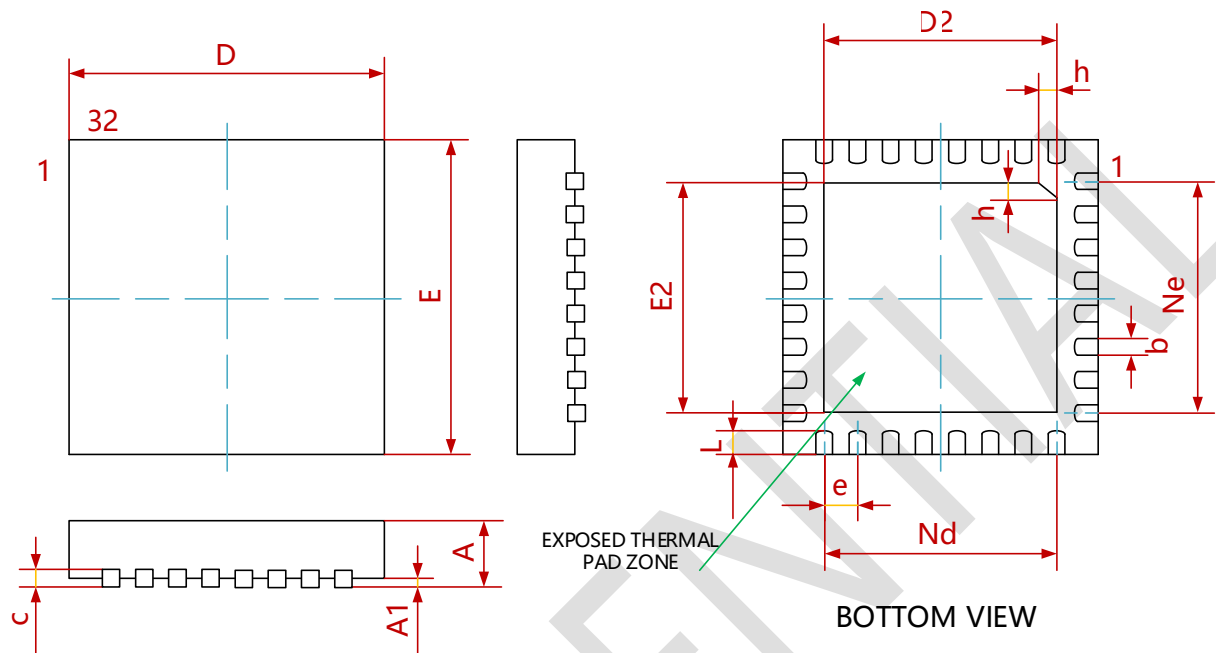
NC = No Connection - should NOT be connected to any signal.

## TYPICAL APPLICATION SCHEMATIC



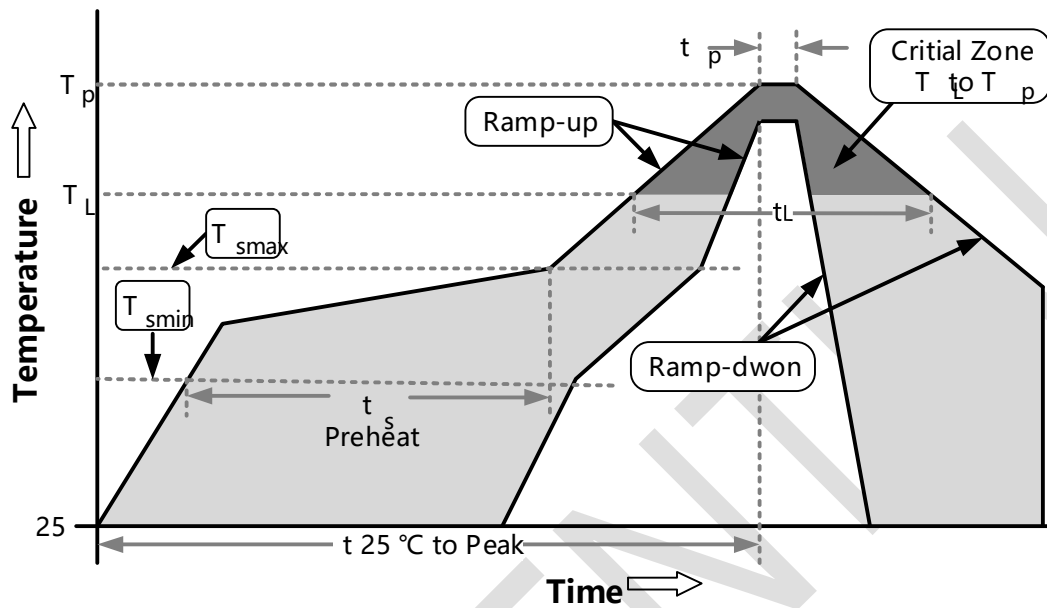
**Notes:** If using external TC/VCXO, CLK should be sent via either pin XI or XO about 1.5V.

## PACKAGE INFORMATION



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Nd	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
Ne	3.50BSC		
L	0.35	0.40	0.45
h	0.30	0.35	0.40

## SOLDER MOUNTING CONDITION



Classification Reflow Profile

Table-I Classification Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T <sub>smax</sub> to T <sub>p</sub> )	3 °C/second max.	3 °C/second max.
<b>Preheat</b>	100 °C	150 °C
-Temperature Min (T <sub>smin</sub> )	100 °C	200 °C
-Temperature Max (T <sub>smax</sub> )	60-120 seconds	60-180 seconds
-Time (t <sub>smin</sub> to t <sub>smax</sub> )		
Time maintained above:	183 °C	217°C
-Temperature (T <sub>L</sub> )	60-150seconds	60-150 seconds
-Time (t <sub>L</sub> )		
Peak /Classification Temperature(T <sub>p</sub> )	See Table-II	See Table-III

Time within 5 °C of actual Peak Temperature (t <sub>p</sub> )	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Table-II SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 ≥ 350
< 2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
≥ 2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table-III Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm3 < 350	Volume mm3 350-2000	Volume mm3 > 2000
< 1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
≥ 2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance: The device manufacturer/supplier <b>shall</b> assure process compatibility up to and including the stated classification temperature (this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

**Note 1:** All temperature refer topside of the package. Measured on the package body surface.

**Note 2:** The profiling tolerance is + 0 °C, - X °C (based on machine variation capability) whatever is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

**Note 3:** Package volume excludes external terminals (balls, bumps, lands, leads) and/or non-integral heat sinks.

**Note 4:** The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may still exist.

**Note 5:** Components intended for use in a “lead-free” assembly process shall be evaluated using the “lead free” classification temperatures and profiles defined in Table-I II III whether or not lead free.

## ROHS COMPLIANT

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC(RoHS).

## ESD SENSITIVITY

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.